25:

E_1	E_2	E_3	C_1	C_2	C_3	u	D
1	0	0	1	X	X	0	0
1	0	0	0	1	X	1	0
1	0	0	0	0	1	1	0
0	0	1	0	0	1	0	0
0	0	1	X	1	0	0	1
0	0	1	1	0	0	0	1
0	0	1	0	1	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	X	1	0
0	1	0	0	0	1	1	0
0	1	0	0	0	0	0	0
X	X	X					

101
choice:
down!

$$u = E_1 \, \bar{C_1} \, (C_2 + C_3) + E_2 \, \bar{C_2} \, \bar{C_1} \, C_3$$

26) a) Not sync as #3 clocked by Q_2

B   C   D
0   0   0
1   1   0 0
JK   JK   SR

→ 1 0 0 → 0 1 0 → 1 1 0
   1 1 0 0   1 1 0 0   1 1 1 0

                              ↓

0 0 0 ← 0 0 1
          0 1 1 1 0 0

b) A toggles
D C B A
0 0 0 0 → 0001 → 0010 → 0011 → 0100 → 0101
                                           ↓
                                        0110
1001 ← 1000 ← 0111 ←

c) D C B A → 0010 → 0100 → 0110
   0 0 0 0   ↓
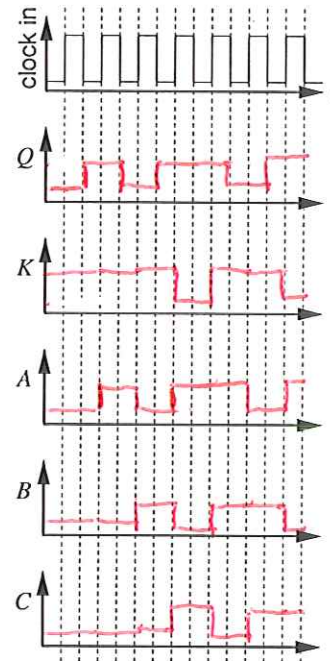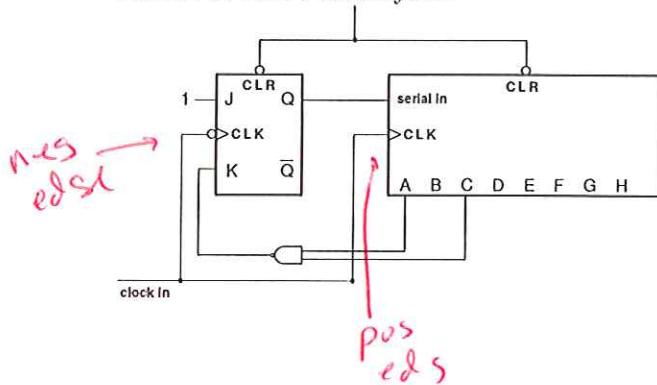   1000
0111 ← 0101 ← 0011 ← 0001 ← 1000
   ↳ 1001 → 0000
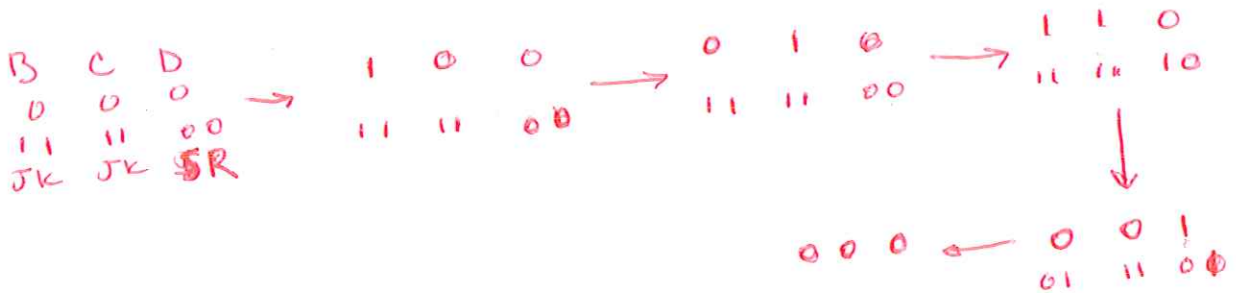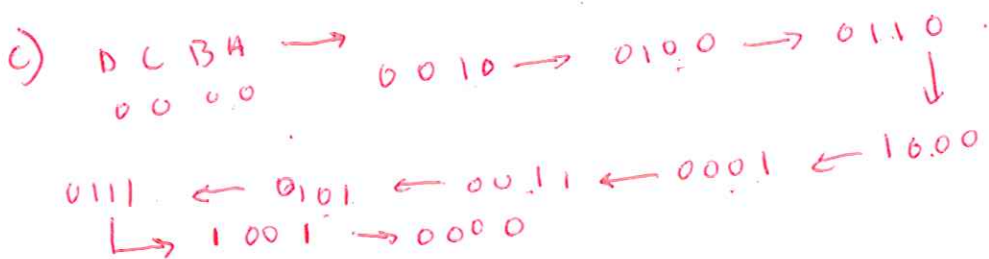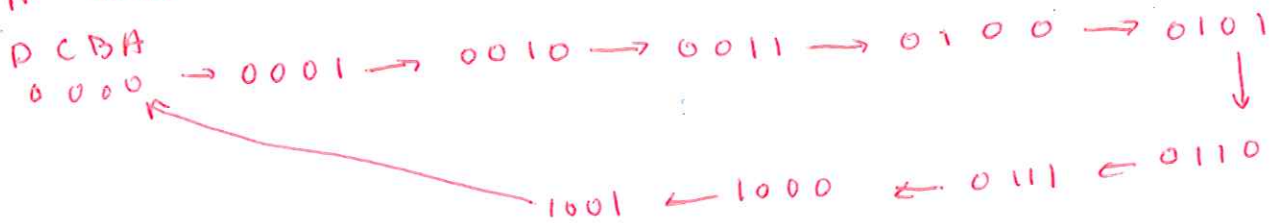
29. Consider the below circuit using pair of JKFF. Directly on this sheet appropriately (i.e., correctly given the circuit diagram) label each JKFF "negative edge triggered" or "positive edge triggered". At the start of this clock sequence Q_1 and Q_2 are both HIGH; controls J_1 and K_1 are changed as shown in the below plot stack and controls J_2 and K_2 are determined by the circuit. Directly on the below stack of output traces record Q_1 (i.e., output of #1 JKFF) and Q_2 for the given "clock in" stream.

J Q
>CLK
K Q̄
#1

J Q
>CLK
K Q̄
#2

clock in

J_1

K_1

Q_1

Q_2

t
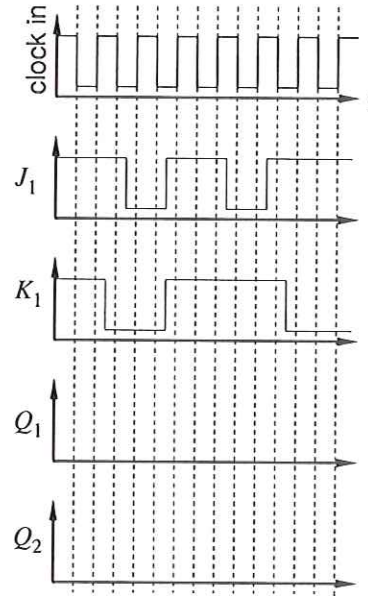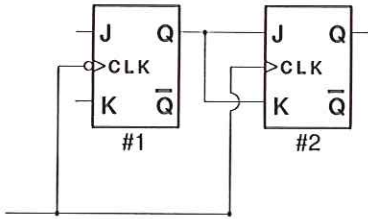
30. Consider the below circuit using a shift register and a JKFF. The chips are cleared and the clock started. Graph (on this page) a stack of output traces: Q, K, A, B, and C underneath the clock input stream. Include at least 7 clock cycles.

CLR
1 — J   Q
  >CLK
   K   Q̄

serial in
CLR
>CLK
A B C D E F G H

clock in

neg edge

pos edg

clock in

Q

K

A

B

C

t

31. For this problem you will need the pinout and function table of the '121 monostable. The required information can be found in Fig. 7.59 HH p. 462 and/or sn74121.pdf (downloaded from ti.com and placed in the class web site). Design circuits (and record exact wiring diagrams—including pin numbers) that do the following:

(a) make a 20 μs pulse on a positive edge

(b) make a 20 μs pulse delayed by 1 ms from a negative edge

(c) make a 50 kHz symmetrical square wave

38. We return here to the problem of finding circuits for state diagrams. Recall that the current state must totally control the following state. But what if we want various futures for a state in various circumstances?
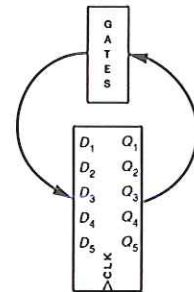
The Morse Code is a bit unusual encoding of letters in that the letters require differing numbers of dot/dashes from one (E=dot=0, T=dash=1) to four (e.g., Q=dash-dash-dot-dash). If we restrict ourselves to the eight letters expressed with 3 bit Morse Code expressions: (D=100, G=110, K=101, O=111, R=010, S=000, U=001, W=011), we can make some odd sentences like: DORKS GROK SORROW. Imagine a circuit that cycles through these letters (i.e., D→O→R→K→S→ etc.). However see that the four Os have different targets: O→R, O→K, O→W. Therefore the *circuit* must distinguish four different types of O (but of course the display will show the same lettershape for each O state). Thus:

$$D \to O_0 \to R_0 \to K_0 \to S_0 \to G \to R_1 \to O_1 \to K_1 \to S_1 \to O_2 \to R_2 \to R_3 \to O_3 \to W$$

Each state will now be labeled with five bits $Q_1 Q_2 Q_3 Q_4 Q_5$ — $Q_3 Q_4 Q_5$ specifying the lettershape and $Q_1 Q_2$ distinguishing the various 'identical' letters. Fill in the below table so it displays the desired cycle and the D_i required to generate it. Find a boolean expression for one of the D_i in terms of the Q_i.
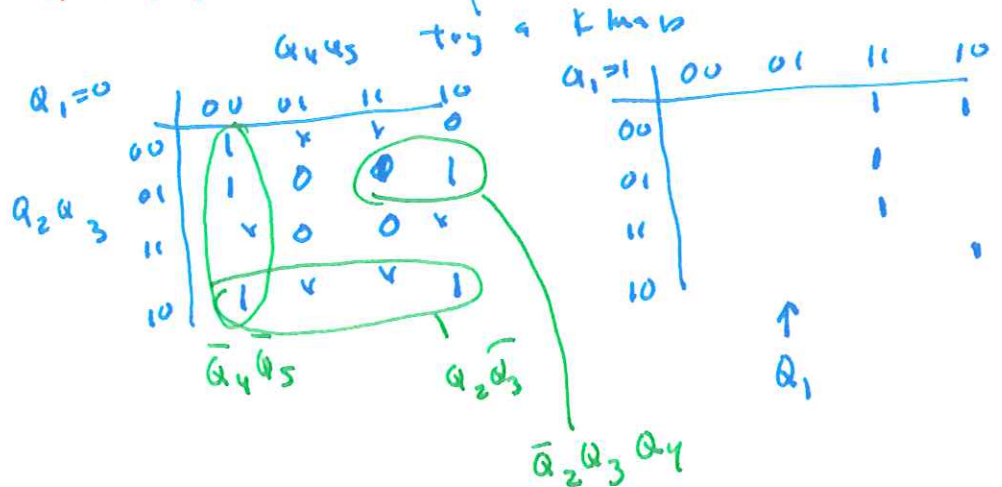
Note: Can always min terms or max term

	Q_1	Q_2	Q_3	Q_4	Q_5	D_1	D_2	D_3	D_4	D_5
D	0	0	1	0	0	0	0	1	1	1
O	0	0	1	1	1	0	0	0	1	0
R	0	0	0	1	0	0	0	1	0	1
K	0	0	1	0	1	0	0	0	0	0
S	0	0	0	0	0	0	0	1	1	0
G	0	0	1	1	0	0	1	0	1	0
R	0	1	0	1	0	0	1	1	1	1
O	0	1	1	1	1	0	1	1	0	1
K	0	1	1	0	1	0	1	0	0	0
S	0	1	0	0	0	1	0	1	1	1
O	1	0	1	1	1	1	0	0	1	0
R	1	0	0	1	0	1	1	0	1	0
R	1	1	0	1	0	1	1	1	1	1
O	1	1	1	1	1	0	0	0	1	1
W	0	0	0	1	1	0	0	1	1	1

39. HH describes more than half a dozen temperature transducers. Pick out three of these and 'compare and contrast' them—that is report their advantages and disadvantages. Describe a situation in a physics lab requiring a temperature measurement and report which transducer you would select and why.

$$\overline{Q_1 \cdot (Q_2 Q_3)} + Q_2 \bar{Q_3} \bar{Q_4}$$

$Q_4 Q_5$ try a k map

$Q_1 = 0$

$Q_2 Q_3$	00	01	11	10
00	1	1	0	1
01	1	1	0	0
11	1	0	0	1
10	1	1	1	1

$\bar{Q_4}\bar{Q_5}$ $Q_2\bar{Q_3}$

$Q_1 = 1$	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

↑ Q_1

$\bar{Q_2} Q_3 Q_4$

$$Q_1 + \bar{Q_4}\bar{Q_5} + Q_2\bar{Q_3} + Q_2\bar{Q_3}Q_4 = D_4$$

48) Mux as ROM — basic idea treat TT inputs as an
    address to the Mux tie the same-number D line
    as required in TT

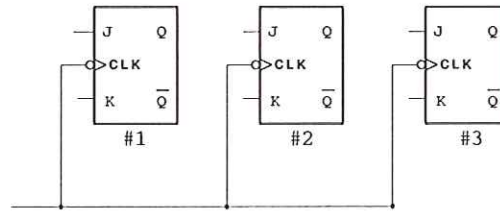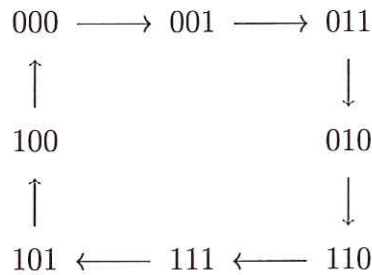| A	B	C	Name	Pin	tre
0	0	0	D0	4	1
1	0	0	D1	3	1
0	1	0	D2	2	1
1	1	0	D3	1	e
0	0	1	D4	15	0
1	0	1	D5	14	1
0	1	1	D6	13	1
1	1	1	D7	12	0

pin 16 = Vcc
pin 8 = GND
pin 7 = strobe = GND

output pin 5 = Y

Note: ABC in problem different
      order from ABC in spec sheet

4. The Gray code state diagram of the three binary digits: $Q_1Q_2Q_3$ is displayed below:

$000 \longrightarrow 001 \longrightarrow 011$

$\uparrow$ $\qquad\qquad\qquad\downarrow$

$100 \qquad\qquad\qquad 010$

$\uparrow$ $\qquad\qquad\qquad\downarrow$

$101 \longleftarrow 111 \longleftarrow 110$

Your job is to design a synchronous circuit built from three edge-triggered JKFFs that follows the above state diagram, where the three binary digits $Q_1Q_2Q_3$ are the outputs of distinct edge-triggered JKFFs. You will need to determine the gate arrangement needed to make this cycle run, i.e., connecting the outputs of the three JKFFs: Q_i to the inputs of the three JKFFs: J_iK_i possibly using the usual (AND, OR,...) gates.

(a) Begin by considering the possible transitions of a single JKFF. What values of JK allow a particular transition? Fill in the below table. Hint: in every row either J or K will be an X for "don't care".

Transition:	J	K
$0 \longrightarrow 0$	0	X
$0 \longrightarrow 1$	1	X
$1 \longrightarrow 0$	X	1
$1 \longrightarrow 1$	X	0

(b) Now fill in the below table which displays the desired cycle.

Q_1	Q_2	Q_3	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	X	0	X	1	X
0	0	1	0	X	1	X	X	0
0	1	1	0	X	X	0	X	1
0	1	0	1	X	X	0	0	X
1	1	0	X	0	X	0	1	X
1	1	1	X	0	X	1	X	0
1	0	1	X	0	0	X	X	1
1	0	0	X	1	0	X	0	K

(c) Gates for J_1, K_1, J_2, and K_2 can be fairly easily generated using two input gates and the outputs of the JKFFs. Pick one of the above (J_1, K_1, J_2, or K_2) and find a simple expression for it in terms of the Q_i and $\overline{Q}_i$. Implement (construct) your expression using simple gates.

$$J_1 = Q_2 \overline{Q}_3$$
$$K_1 = \overline{Q}_2 \overline{Q}_3$$

$$J_2 = Q_1 \overline{Q}_3$$
$$K_2 = Q_1 Q_3$$

5. The rear turn indicators on old Ford Thunderbirds had a distinctive pattern in which the four segments of the indicator were illuminated sequentially, "pointing" the direction of the turn. For example, on a right-turning T-bird you would see the four segments which made up the right-rear indicator cycle as shown below:
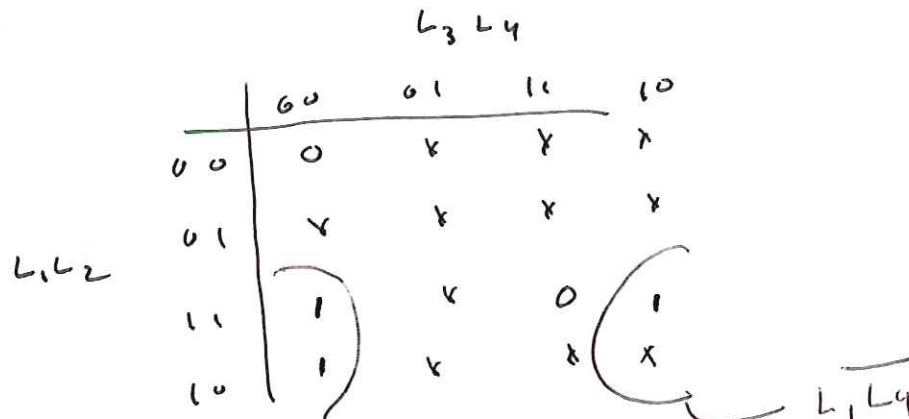
T bird right turn:

clock cycle
○ ○ ○ ○ 1
✳ ○ ○ ○ 2
✳ ✳ ○ ○ 3
✳ ✳ ✳ ○ 4
✳ ✳ ✳ ✳ 5
L_1 L_2 L_3 L_4
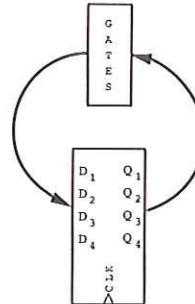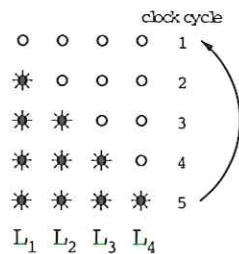
Implement this cycle using four DFFs and external gates ($Q_i = L_i$).

(a) Draw the state diagram for this process.

(b) Display in the below table the desired cycle
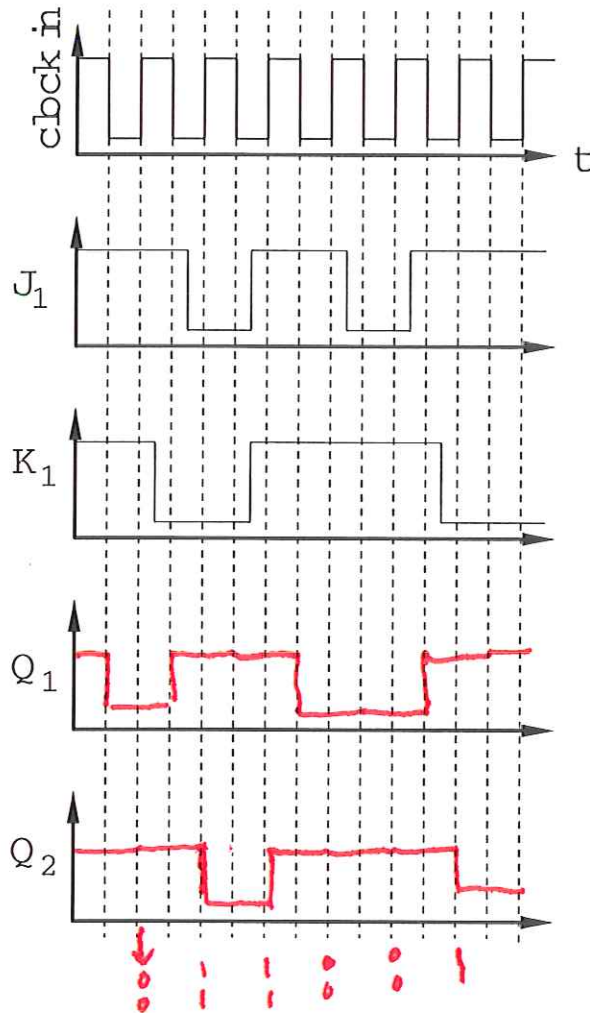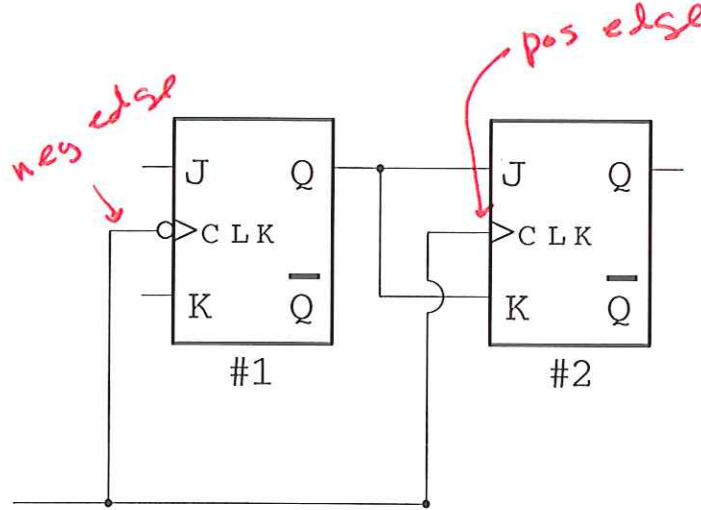
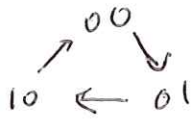| L_1	L_2	L_3	L_4	D_1	D_2	D_3	D_4
0	0	0	0	1	0	0	0
1	0	0	0	1	1	0	0
1	1	0	0	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

(c) Make a Karnaugh map for D_2 in terms of the four logical variables L_1, L_2, L_3, L_4. Note that there will be *lots* of Xs (don't care) entries. Circle appropriate groups to find a boolean expression for D_2. Please carefully label your Karnaugh maps so I know what each row and column of the map represents!

$L_3 L_4$

	00	01	11	10
00	0	X	X	X
01	X	X	X	X
11	1	X	0	1
10	1	X	X	X

$L_1 L_2$

$L_1 L_4$

6. Consider the below circuit using pair of JKFF. Directly on this sheet appropriately (i.e., correctly given the circuit diagram) label each JKFF "negative edge triggered" or "positive edge triggered". At the start of this clock sequence Q_1 amd Q_2 are both HIGH; controls J_1 and K_1 are changed as shown in the below plot stack and controls J_2 and K_2 are determined by the circuit. Directly on the below stack of output traces record Q_1 (i.e., output of #1 JKFF) and Q_2 for the given "clock in" stream.
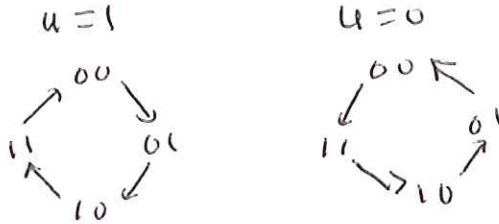
HH 10.23

(state diagram: 00 → 01 → 10 → 00)

	J K
0 →0	0 X
0 →1	1 X
1 →0	X 1
1 →1	X 0

Q_2 Q_1	J_2 K_2	J_1 K_1
0 0	0 X	1 X
0 1	1 X	X 1
1 0	X 1	0 X

Q_1 $\overline{Q_2}$

1 1	1 1	0 1
0 0		

10.24

u = 1   u = 0

(state diagrams and circuit with flip-flops #2 and #1)

clock

u	Q_2 Q_1	J_2 K_2	J_1 K_1
1	0 0	0 X	1 X
1	0 1	1 Y	X 1
1	1 0	X 0	1 X
1	1 1	X 1	X 1
0	0 0	1 X	1 X
0	1 1	X 0	X 1
0	1 0	X 1	i X
0	0 1	0 X	X 1

$\overline{u} \oplus Q_1$ All High