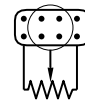
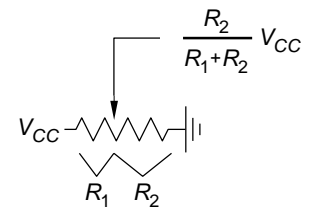


Basic TTL Gates
Serial and Parallel Binary Numbers

0. You will need about ten short (1–2”) connecting wires in both red and black, and at least twelve longer ‘signal’ wires in other colors. For this class you must adopt two consistent practices: (A) color code your wires using red = +5 V (power, V_{CC}), black = 0 V (ground), and other colors for signal wires; and (B) always place chips with pin 1 up (and to the left). Please note that our color code is *not* that used for (120 V, 60 Hz) household wiring; there black is power and white is ground.

The pot or potentiometer (used first in #3 below) is the most common item on the protoboard to be destroyed by students. A pot consists of a sweeper arm (denoted by the arrow) that touches a resistive slab at an adjustable location, dividing the resistive slab into two ‘resistors’. If the ends of the pot are connected to power and ground (see right), the sweeper samples the voltage in between the the ends; the voltage divider equation could be applied to give the sweeper voltage, but in practice neither R_1 or R_2 is known (although they could perhaps be estimated based on how far the pot had been turned). Pots are labeled with the total slab resistance $R_1 + R_2$. On the protoboard, the sweeper is connected to the central four holes. To destroy a pot, all you need do is connect power and ground between the sweeper and an end, and then rotate the knob for small resistance between them; a huge current will flow, burning off the delicate sweeper end. Never draw appreciable current from a sweeper!



- Starting in the upper right, press in the following TTL chips: 7400 (quad NAND), 7402 (quad NOR), 7404 (hex INVERTER), 7408 (quad AND), 7432 (quad OR), 7486 (quad XOR). Record in your notebook the exact chip number of each chip used. (I.e., your chip might be a 74ALS00 or an “equivalent” military chip: /30001.) Note that you will lose points if you do not follow this practice in this and all future labs (i.e., always include a ‘Parts List’ in your notebook). In this particular lab the answers to the below questions will depend on exactly what chip you’re using—so here the grader needs to know. However, since you must return each chip to its proper drawer, a recorded translation between the part number on the chip and the label on the drawer will make finding the proper drawer fast. The ‘pin-out’ diagrams for these chips may be found on the following pages. Connect up power (red) and ground (black) “at the corners.” Pick out one of the two-input gates to check-out. “Fan out” (i.e., connect in parallel) a “side-board” data-switch output to an LED and to a gate input. Do the same for the other gate input using an adjacent data-switch and LED. Display the gate output on a third LED. Check all combinations of gate inputs and record the results in a truth table for the gate. Totally disconnect a chip input and report how the chip interprets (i.e., as H or L) an open (i.e., unconnected) input. Move your circuit over to a gate on a different chip and record the truth table for this new gate. Check out and record the truth table for a third gate.
- Take the wire connected to the output of your gate (whose inputs are still controlled by the side-board switches) and connect it to the input of some other gate. (No other connections please! This is obviously the usual thing to do: connect outputs to inputs.) Using a DMM find the current that flows through this output-to-input wire when the output is high and when the output is low. (Surprised?) Similarly, using a DMM find the voltage (relative to

- ground) of this output-to-input wire in both output states. (When you record the results of a DMM measurement, you should always draw the circuit schematic and display exactly how the measurement was made. For this class measurement errors need not be recorded, but get in the habit of recording every digit displayed by the DMM.)
3. Wire up your right-hand ($1\text{ k}\Omega$) pot with ends at $+5\text{ V}$ and ground. Set the voltmeter to read the voltage on the sweeper, and input the sweeper voltage to an inverter. (You have now made a voltage divider, and you can adjust the sweeper voltage by turning the pot's knob.) Examine the inverter output with the scope. Find the range of input voltages considered by the inverter to be high and low. Compare to the values recorded in the book for the particular type of TTL chip you are testing. (See S 12.4.3–5; or HH Table 9.1 and Figure 9.3b)
 4. Daisy-chain all 6 inverters (i.e., connect output of inverter N to input of inverter $N + 1$ making a chain). Convert 4 additional gates to inverters and add them to the chain. Drive the chain with the function generator (on TTL!). (A TTL pulse output, like that produced by the function generator, is often called a “clock”. The verb “clock” means to drive a circuit with such a signal.) Use the scope to display both the input and the chain output. Sketch the results in your notebook. (Note: when I ask you to make a measurement with a scope, please sketch the scope trace in your notebook and record the *scales* for both axes and the location of ground on the vertical axis. Draw the circuit and show exactly how the scope was connected to the circuit.) Measure the time delay when clocking at maximum speed and compare to typical TTL gate delays. XOR the clock and chain output. Sketch the resulting scope trace. If the clock and chain output were synchronized, the XOR output would be flat. (Why?) The “glitch” in XOR output results from gate delay.
 5. Disconnect the chain input from the function generator and instead drive the chain with the 9^{th} inverter output. What does the chain output look like in the scope? (Of course, sketch the results in your notebook.) Explain!
 6. Design a majority-rule voting system for a committee of three members. Each member is provided with a yes/no switch; an LED lights if and only if the vote passes. Diagram your circuit in your notebook, wire it up, and show your instructor that it works.
 7. Remove the simple gate chips. Wire-up the 7483 (ADDER) using the supplied pin out. This chip adds the 4-bit binary number $A_4A_3A_2A_1$ to the 4-bit binary number $B_4B_3B_2B_1$ to produce a 4-bit sum $\Sigma_4\Sigma_3\Sigma_2\Sigma_1$ and C_{OUT} . (What should you do with C_{IN} ?) The A inputs should be controlled by consecutive side-board data switches; the B inputs will fill out the remaining side-board data switches. Display the 4-bit output and C_{OUT} on consecutive LEDs. Check-out the 7483's operation. Record (in both base 10 and binary) at least three correct 4-bit binary sums $A + B = \Sigma$. For these parallel binary numbers, different wires carry different bits of the number.
 8. Go to room 114 and examine the output of a terminal on a scope. (Connect pin 7 to ground; find the signal on pin 2 for this RS-232 plug.) Hold down a key and sketch the waveform produced. (Repeat this several times.) Describe exactly how the signal displayed by the scope can be translated into the ASCII integer for the key pressed (find ASCII codes in Table 10.3 HH p.721 or S p.637) . Note carefully the starting bits and stopping bits. Is the MSB of the ASCII integer on the left or right side of the scope display? Find the voltages that correspond to logical 1 and logical 0. (Surprised?) Figure the baud rate (bits per second) from the scope and compare to the set value (9600 baud). Make sure you include several carefully sketched scope waveforms that show where each bit of the ASCII integer is in the scope trace.
 9. **Advice:** Retain this (and future) lab descriptions as the attached chip pin-outs will aid you in your digital design project (Lab 6).