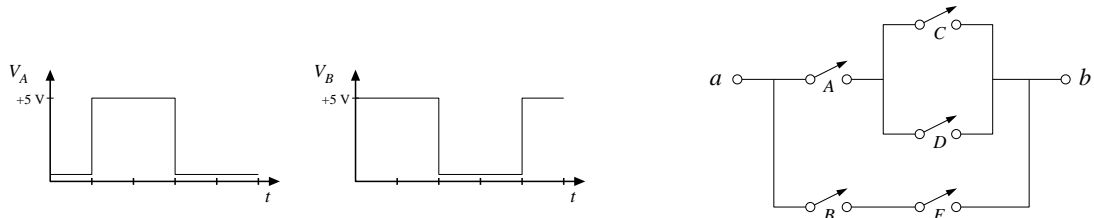
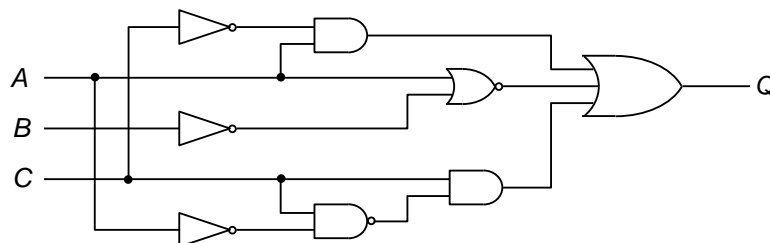


- Answer the following questions on number systems. (Ref. S 12.1.2 & HH 8.03)
  - Convert the following decimal numbers to binary: 28, 100, and 341
  - Convert the following sequence of decimal numbers to binary: 15, 16, 17, 18, 19
  - Convert the following binary numbers to decimal: 1101, 10101010, and 1111
  - Convert the above binary numbers to octal.
  - Convert the above binary numbers to hexadecimal
  - Convert  $365_{10}$  to BCD
  - Convert the BCD number 0100,0001 to binary.
- Without converting to decimal, directly add the following binary numbers. Then check your answers by converting each number to decimal.
  - $111011 + 101110$
  - $01011 + 110$
  - $010101 + 01101$
- Voltages  $V_A$  and  $V_B$  (plotted below left as functions of time) are used as inputs to simple gates. Graph the gate output as a function of time if the gate is:
  - AND (i.e.,  $V_A \cdot V_B$ )
  - OR (i.e.,  $V_A + V_B$ )

You have probably answered this question assuming positive-true (S p. 632, HH p. 472 + 8.07) logic. Answer again assuming negative-true logic.



- Consider the switch network shown above right. Deduce the Boolean expression for the condition that the circuit conducts current between  $a$  and  $b$ . (A closed switch is to be considered true.)
- Consider the below mess of gates:

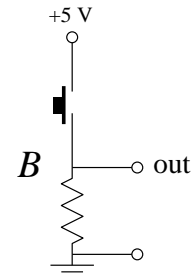
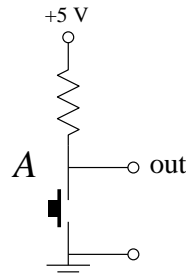
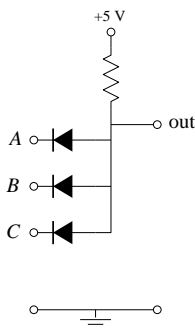


- Convert the mess of gates into the equivalent boolean expression.
  - Use boolean algebra to reduce your boolean expression.
  - Express your reduced expression in gates.
  - Draw this circuit and label the logic level of every wire assuming  $(A, B, C) = (0, 0, 0)$ .
- The statement “ $A$  or  $B$  and  $C$ ” can be interpreted in two ways. Write unambiguous Boolean expressions for each interpretation and express the resulting expression in a circuit of simple gates.

7. Go to the Texas Instruments web site ([www.ti.com](http://www.ti.com)) and find the data sheet for a 7400 (quad NAND gate). Print out the first page (which should show the pinouts for the various packages). Go to the Digi-Key web site ([www.digikey.com](http://www.digikey.com)) and find the part number and price for a 7400 in the 14 pin DIP package.

8. Consider the diode-logic circuit with inputs  $A$ ,  $B$  and  $C$  shown below left.

- Suppose  $C$  is brought low by connecting it to ground, while  $A$  and  $B$  unconnected. What is the output voltage?
- Suppose  $C$  is brought low by connecting it to ground, while  $A$  and  $B$  remain connected to +5 V. What is the output voltage?
- Suppose both  $B$  and  $C$  are held low by connecting it to ground, while  $A$  is connected to +5 V. What is the output voltage?
- What logic function is implemented by this circuit?
- Suppose  $C$  is brought low by connecting it through a  $1\text{ k}\Omega$  resistor to ground, while  $A$  and  $B$  remain connected to +5 V. What is the output voltage?



9. Consider two possible designs for a push-button controlled logic level as diagrammed above right. In design A, a NO SPST push button (HH p. 54, S p. 304) is connected to +5 V via a resistor ('pull-up resistor'). In design B, a NO SPST push button is connected ground via a resistor ('pull-down resistor'). What problems result (in each case) if  $R$  is made too-large? What is a proper choice for  $R$  (approximately for each case)? Generally speaking which design is superior for TTL gates? Report why.
10. Design a majority-rule voting system for a committee of three members. Each member is provided with a yes/no switch; the output is true if and only if the vote passes. Your design should include both a circuit of simple gates implementing the function and the corresponding Boolean expressions.
11. (a) Show that  $A + \overline{A}B = A + B$  using two of the following three methods: Venn Diagram, complete enumeration of all cases in a truth table, or by Boolean algebra.
- (b) Show:
- $$\overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} = \overline{A \cdot B}$$
- (c) Directly implement each side of this expression in gates. How many gates are saved by using the reduced form?
12. (a) Consider
- $$T = (A + B)(\overline{B} + A)$$
- Draw the gate circuit that follows directly from this statement.
- (b) Assume  $A = 1$  and  $B = 0$ . Directly on your circuit diagram, label the logic level of each wire.
- (c) Reduce the Boolean expression for  $T$ . Show that your reduced expression in fact produces the same output as the full expression with the inputs  $A = 1$  and  $B = 0$ .

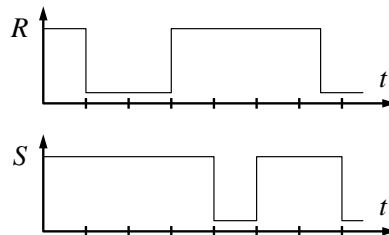
13. Reduce the following expressions:

- (a)  $\overline{A} \cdot \overline{((B \cdot C) + B)} \cdot \overline{A}$
- (b)  $\overline{AB} + (A + \overline{B})$
- (c)  $(A + AB) + \overline{AB}$
- (d)  $(\overline{A} + \overline{B})(A \cdot \overline{B})$
- (e)  $[(AB + A\overline{B}) + AB] + \overline{AB}$

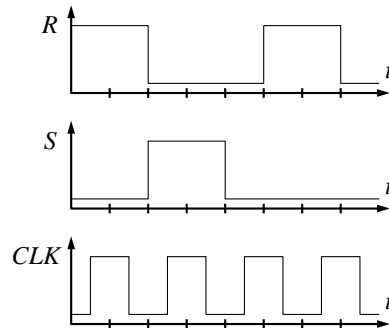
14. (a) Write the sum-of-products (minterm) expression for this truth table.  
 (b) Write the product-of-sums (maxterm) expression for this truth table.

| <i>A</i> | <i>B</i> | <i>C</i> | <i>T</i> |
|----------|----------|----------|----------|
| 0        | 0        | 0        | 0        |
| 0        | 0        | 1        | 1        |
| 0        | 1        | 0        | 0        |
| 0        | 1        | 1        | 1        |
| 1        | 0        | 0        | 1        |
| 1        | 0        | 1        | 0        |
| 1        | 1        | 0        | 0        |
| 1        | 1        | 1        | 0        |

15. Consider the cross-NAND SR FF with *S, R* inputs (plotted as a function of time) as shown below. Graph *Q* (along with *R, S*) as functions of time. (The graphs for this and the following problems should be ‘stacked’, as in the below examples, so that the simultaneous behavior of all the signals can be assessed.) Note: S p. 682 has the correct truth table but wrong circuit and output trace (essentially *Q* and  $\overline{Q}$  are switched). HH Fig. 8.47 is a cross-NAND SR FF, but ‘bubble pushing’ has moved the invert to the inputs with AND→OR.

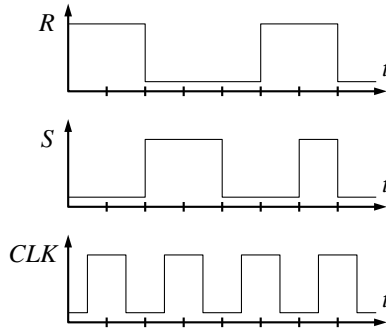


16. Consider the level-triggered cross-NAND SR FF (HH Fig. 8.51 or S p. 684) with *S, R, CLK* inputs (plotted as a function of time) as shown below. Graph *Q* (along with *R, S, CLK*) as functions of time.



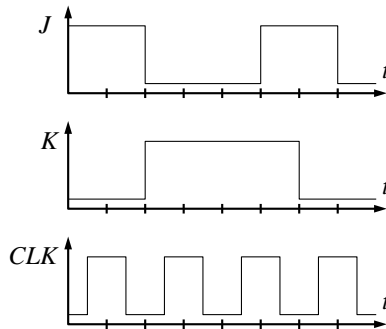
17. Consider the edge-triggered cross-NAND SR FF (S p. 685) with  $S, R, CLK$  inputs (plotted as a function of time) as shown below. Graph  $Q$  (along with  $R, S, CLK$ ) as functions of time for:

- (a) positive edge triggered SR FF
- (b) negative edge triggered SR FF



18. Consider the edge-triggered JK FF (HH p. 509 or S p. 691) with  $J, K, CLK$  inputs (plotted as a function of time) as shown below. (Note: essentially all JK truth tables in S incorrectly show the SET and RESET as resulting in  $(Q\bar{Q}) = (00)$ .) Assume that initially  $Q = 0$ . Graph  $Q$  (along with  $J, K, CLK$ ) as functions of time for:

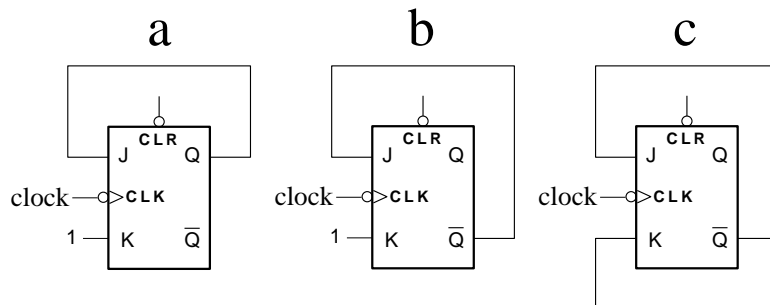
- (a) positive edge triggered JK FF
- (b) negative edge triggered JK FF



19. A new type of controlled flip-flop satisfying the below state table is required for a design. Show how you can make this FF from a JKFF an a few simple gates.

| $A$ | $B$ | $Q_{n+1}$   |
|-----|-----|-------------|
| 0   | 0   | $\bar{Q}_n$ |
| 1   | 0   | $Q_n$       |
| 0   | 1   | 0           |
| 1   | 1   | 1           |

20. For each of the following circuits, assume that initially  $Q = 0$  and then a series of clock pulses are applied to  $CLK$ . For each circuit plot  $Q$  and  $CLK$  as functions of time.

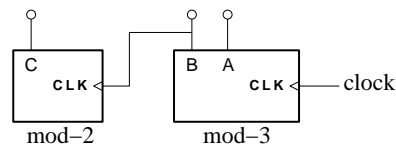


21. (a) A simple indicator of minimum overnight temperature is desired. Assume that three normally open SPST switches are available that close when the temperature falls below  $10^{\circ}\text{C}$ ,  $5^{\circ}\text{C}$ , and  $0^{\circ}\text{C}$ . (The switches open again when the temperature rises above the set point.) Design an instrument with three light indicators; each indicator lights and holds if the temperature falls below its set point. A reset button should be provided so that the instrument can be cleared after reading it the following morning. Assume that the indicator lights operate using the usual logic level voltages (HIGH=light on, LOW=light off).
- (b) In a conventional mercury thermometer a column of mercury moves up or down responding to the current temperature. Design an instrument in which a column of lighted lights acts like the mercury column: additional lights lighting (lengthening the lighted column) as the temperature rises. Assume that 30 switches are available with set points in increments of  $1^{\circ}\text{C}$  (i.e.,  $0^{\circ}\text{C}$ ,  $1^{\circ}\text{C}$ ,  $2^{\circ}\text{C}$ ,  $\dots$ ,  $29^{\circ}\text{C}$ ).
22. A building has a turnstile for incoming people and another turnstile for people leaving the building. The output of a turnstile is generally HIGH but, when a person passes through it, a short ( $\sim 100\text{ ns}$ ) LOW pulse is produced. Show how, with a just a handful of extra gates, a 74191 can be used to display the number of people actually in the building. Note: S p. 705 describes the 74193 counter which exactly solves this problem: a counter with separate up and down clock inputs, but you are instead to use the '191 described S p. 706 and used in Lab 3. The first thing you must do is combine the two turnstile outputs to make one clock—you may assume that the pulses are so short that they *never* overlap. Next you need to figure out how to control the '191's  $\overline{U}/D$  pin.
23. A crossed-NAND SR FF has an active low Set pin ( $S \rightarrow 0 \Rightarrow Q \rightarrow 1$ ) and an active low Reset (clear) pin ( $R \rightarrow 0 \Rightarrow Q \rightarrow 0$ ). The setting and clearing action is immediate: there is no clock. A D FF has a Data pin ( $D$ ), the value of which is read and transferred to the output when the Load pin ( $L$ ) goes high. Consider the process of making a D FF from a SR FF and some additional gates. The Load and Data lines must somehow control the Set and Reset pins to make the SR FF act as desired.

- (a) Begin by thinking what  $S$  and  $R$  need to be for all possible combinations of  $D$  and  $L$ . This is best done by completing the truth tables:

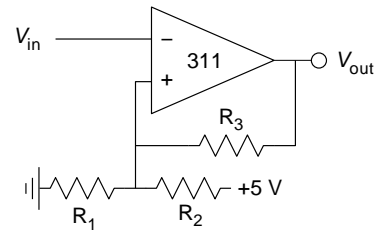
| $D$ | $L$ | $S$ | $D$ | $L$ | $R$ |
|-----|-----|-----|-----|-----|-----|
| 0   | 0   |     | 0   | 0   |     |
| 1   | 0   |     | 1   | 0   |     |
| 0   | 1   |     | 0   | 1   |     |
| 1   | 1   |     | 1   | 1   |     |

- (b) Write down the Boolean expression for each truth table.
- (c) Draw the circuit required for  $D$  and  $L$  to drive  $R$  and  $S$ .
24. A mod-3 counter (e.g., HH Fig. 8.60 p. 514 with output digits  $BA$ ) and a mod-2 counter (e.g., a toggling FF with output digit  $C$ ) are connected together as shown below. Graph the  $C, B, A$  outputs for a square wave clock input. Show that  $C$  is a symmetrical square wave with a frequency  $1/6$  of the input frequency. Assume that both counters are synchronous, but with an output delay of  $30\text{ ns}$ . What cycle of  $C, B, A$  states is actually produced by this asynchronous connection?



25. An elevator services three floors of a hotel. There are three logical variables:  $E_1, E_2, E_3$ , which record the floor at which the elevator sits.  $E_i = 1$  if the elevator is on the  $i^{\text{th}}$  floor and is 0 otherwise. (For example, if the elevator is on the 2<sup>nd</sup> floor,  $E_2 = 1$  while  $E_1 = E_3 = 0$ . Assume exactly one of the  $E_i$  will be 1.) On each floor there is an elevator call button. The logical variables  $C_1, C_2, C_3$  record unsatisfied requests for elevator service.  $C_i = 1$  if the elevator is requested on the  $i^{\text{th}}$  and is 0 otherwise. (For example, if  $C_2 = 0$  while  $C_1 = C_3 = 1$ , the elevator is requested on the first and third floors.) In responding to call requests the elevator can go up (if up-motor control  $U=1$ ) or down (if down-motor control  $D=1$ ) or not move (if  $U=0$  and  $D=0$ ). ( $U=1$  and  $D=1$  should never occur.) Write a logical expression for  $U$  as a function of inputs  $E_i$  and  $C_i$ . Do the same for  $D$ . Your answer should represent rational elevator behavior; for example the elevator must answer the *closest* call request.
26. The logic circuit for a 7490 (shown below, also see S p. 704) involves negative edge triggered JK FF and RS FF. Each of the FF has asynchronous (direct) set ( $S_D$ ) and re-set (clear) ( $R_D$ ) inputs.
- Graph the important signals as a function of time to show that  $Q_1, Q_2, Q_3$  and  $C_{p1}$  form a Mod-3 counter.
  - What is the output if  $MS_1$  and  $MS_2$  are both HIGH?
  - If  $Q_0$  is connected to  $C_{p1}$  and the device is clocked on  $C_{p0}$ , what output result? Explain and graph the output of the important signals.
  - If  $Q_3$  is connected to  $C_{p0}$  and the device is clocked on  $C_{p1}$ , what output result? Explain and graph the output of the important signals.

27. Consider the classic Schmitt<sup>1</sup> trigger circuit, where you can assume that the output of the 311 swings between +5 V and 0 V. (This need not actually be the case; for example, the 311 would require a pull-up resistor.) Design a circuit which has transitions at +1.0 V and +1.5 V. As you recall, when the 311's output is low we have a voltage divider with  $R_1 \parallel R_3$  and  $R_2$  whereas when the 311's output is high we have a voltage divider with  $R_1$  and  $R_2 \parallel R_3$ . The difference between these two,  $\Delta V$ , is given by a voltage divider with  $R_1 \parallel R_2$  and  $R_3$ .



The above question has some difficulties. First it requests three answers ( $R_1, R_2, R_3$ ) from two equations (the two set-point voltages). Systems of equations with more unknowns than equations cannot in general be solved. (They are called underdetermined.) While mathematicians may not approve of such problems, they occur all the time in real life. They are what “design” is all about: options to be selected. In this question if  $(R_1, R_2, R_3)$  is a solution then so is  $(xR_1, xR_2, xR_3)$ , for any multiplier  $x$ . Design here then amounts to setting an overall scale for the resistors. “Reasonable”<sup>2</sup> resistor values are often in the range  $k\Omega$  to  $M\Omega$ . Furthermore, actual for-sale resistors come in a limited range of values (see HH p. 1053). A second problem has to do with the non-linear nature of the equations for the set-point voltages. A practical (‘trial and error’) way of solving these equations is to find the  $R_3/(R_1 \parallel R_2)$  that produces the the desired level of hysteresis ( $\Delta V$ ) and then use the simple voltage divider equation (for a voltage in the suggested range) to relate  $R_2$  and  $R_1 \parallel R_2$ . Once the  $R_i$  have been found you can use the exact equations to determine the actual switching points. This results in fairly simple algebra, and usually works adequately (if not just iterate the process). *Mathematica*, of course, can provide an immediate exact solution. . .

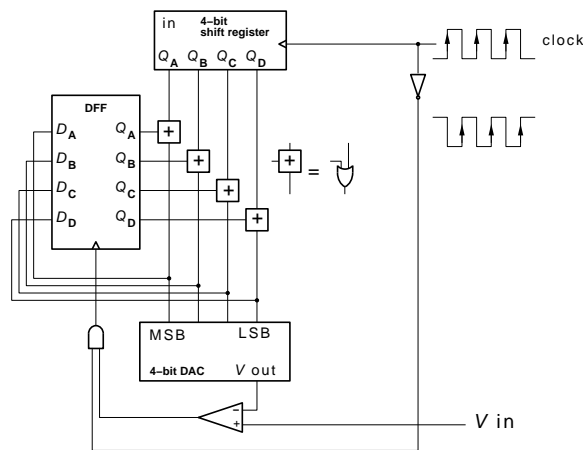
Solve[{1.5/5==r1/(r2 r3/(r2+r3)+r1) , 1./5==r1 r3/(r1+r3)/(r1 r3/(r1+r3)+r2)}, {r1,r2}]

- Make a design using *Mathematica*.
- Made a design using the approximate approach.

<sup>1</sup>Otto Herbert Schmitt 1923–1998; Ph. D. 1937 Washington University (St. Louis) (physics, zoology), UMn Bio-Physics prof 1941–98

<sup>2</sup>“Small” resistors may lead to large power loss:  $V^2/R$ ; “large” resistors are more susceptible to noise and stray capacitance problems.

28. For this problem you will need the pinout and function table of the '121 monostable. The required information<sup>3</sup> can be found in Fig. 8.64 HH p. 518 and/or [sn74121.pdf](#) (downloaded from [ti.com](#) and placed in the class web site). Design circuits (and record exact wiring diagrams) that do the following:
- make a 20  $\mu\text{s}$  pulse on a positive edge
  - make a 20  $\mu\text{s}$  pulse delayed by 1 ms from a negative edge
  - make a 50 kHz symmetrical square wave
29. Refer to the 74121 pinout function table described in the previous problem and answer the following multiple choice questions:
- If  $A_1$  and  $B$  are high, the monostable will produce a pulse if:
    - $A_2$  goes low to high
    - $A_2$  goes high to low
    - neither as it is inhibited
  - If  $A_1$  is low and  $B$  is high, the monostable will produce a pulse if:
    - $A_2$  goes low to high
    - $A_2$  goes high to low
    - neither as it is inhibited
  - If  $A_1$  and  $B$  are low, the monostable will produce a pulse if:
    - $A_2$  goes low to high
    - $A_2$  goes high to low
    - neither as it is inhibited
  - If  $A_1$  is low and the voltage on  $A_2$  is unknown, the monostable will produce a pulse if:
    - $B$  goes low to high
    - $B$  goes high to low
    - it depends on the voltage on  $A_2$
30. Consider a cartoon version of a 4-bit successive approximation ADC:



Assume that controls not shown on the diagram arrange that at the start of a conversion the DFF and shift register are cleared and then one 1, starting in  $Q_A$ , shifts to the right through the shift register. Assume the DAC is perfectly linear, producing  $V_{\text{out}} = \frac{1}{3}$  digital in, i.e., +5 V out for an input of  $15 = 1111_2$  (and 0 V out for input of 0). Graph the DAC output during the conversion if  $V_{\text{in}} = 3.14$  V. Graph the DAC output during the conversion if  $V_{\text{in}} = 2.99$  V. What is the smallest  $V_{\text{in}}$  that results in a digital output of 1? Carefully compare the ideal ADC curve (HH Fig. 9.44A, p. 615) to what would result with this ADC. What is the difference?

<sup>3</sup>Fig. 12.94 p. 698 S is potentially useful if you recognize that: the pin labeled  $\overline{A_1}$  in S is exactly the same pin as that labeled  $A_1$  in HH and [sn74121.pdf](#), and the bottom two rows on the truth table are wrong. They should read

(as they do in HH and [sn74121.pdf](#)):

| $A_1$ | $A_2$ | $B$        | $Q$       | $\overline{Q}$ |
|-------|-------|------------|-----------|----------------|
| L     | X     | $\uparrow$ | $\square$ | $\sqcup$       |
| X     | L     | $\uparrow$ | $\square$ | $\sqcup$       |



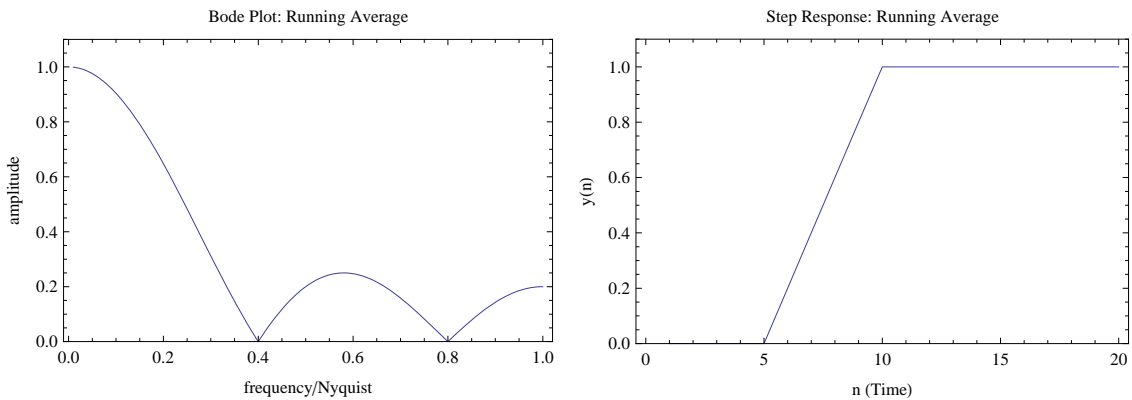
34. HH describes more than half a dozen temperature transducers. Pick out three of these and 'compare and contrast' them—that is report their advantages and disadvantages. Describe a situation in a physics lab requiring a temperature measurement and report which transducer you would select and why.
35. A running average (of five) digital filter would be described by the equation:

$$y_n = \frac{1}{5} (x_n + x_{n-1} + x_{n-2} + x_{n-3} + x_{n-4})$$

Let  $x_n$  be a unit step that occurs at  $n = 6$ , i.e.,

$$x_n = \begin{cases} 0 & n < 6 \\ 1 & n \geq 6 \end{cases} \quad \text{where you are to assume: } y_n = 0 \text{ for } n < 6$$

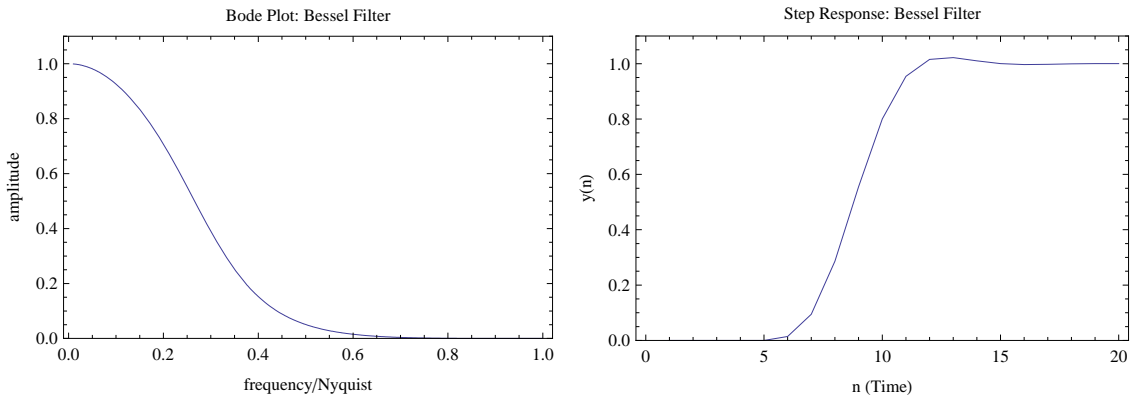
The below right shows the resulting response ( $y_n$ ) to this unit step input. The below left shows a Bode plot: the equilibrium  $y_n$  amplitude when the input  $x_n$  is a unit-amplitude sinusoid with frequency  $f$ . (The  $x$  axis is  $f$  divided by the Nyquist frequency.)



A fourth order Bessel digital filter would be described by the equation:

$$y_n = \frac{1}{68.94} (x_n + 4x_{n-1} + 6x_{n-2} + 4x_{n-3} + x_{n-4}) - 0.05034y_{n-4} + 0.3599y_{n-3} - 1.0459y_{n-2} + 1.5042y_{n-1}$$

The below right shows the resulting response ( $y_n$ ) to the unit step input. The below left shows a Bode plot: the equilibrium  $y_n$  amplitude when the input  $x_n$  is a unit-amplitude sinusoid with frequency  $f$ . (The  $x$  axis is  $f$  divided by the Nyquist frequency.)



- Calculate  $y_7$  for both filters.
- If the sampling rate is 10000 Hz, what is the Nyquist frequency?
- If the input is a unit-amplitude sinusoid with frequency  $f = 2500$  Hz, use the above graphs to find the resulting  $y$  amplitude for both filters.

## 36. Vocabulary

- A. CMOS, TTL
- B. DIP
- C. VLSI
- D. Tri-state (Hi-Z)
- E. pull-up resistor
- F. logic probe
- G. gate delay
- H. glitch
  - I. fan-out
- J. wired OR
- K. two's complement
- L. decoder
- M. encoder
- N. multiplexer (MUX)
- O. demultiplexer (deMUX)
- P. RSFF
- Q. JKFF
- R. DFF
  - S. synchronous
- T. ripple counter
- U. shift register
- V. maxterm (POS), minterm (SOP)
- W. Bus
  - X. state diagram
  - Y. PLA or PAL
  - Z. FPGA
- a. ROM, PROM, EPROM
- b. RAM (D & S)
  - c. address
  - d. register
  - e. stack
  - f. stack pointer
  - g. program counter
- h. BCD
  - i. ASCII
  - j. baud
  - k. byte, nibble
  - l. comparator
- m. Schmitt trigger
- n. hysteresis
- o. monostable
- p. VCO
- q. transducer
- r. DAC
- s. dual-slope ADC
- t. successive approximation ADC
- u. flash ADC
- v. DSP
- w. FFT
- x. Bode plot
- y. Nyquist frequency
- z. FIR & IIR digital filters