Field Effect Transistors

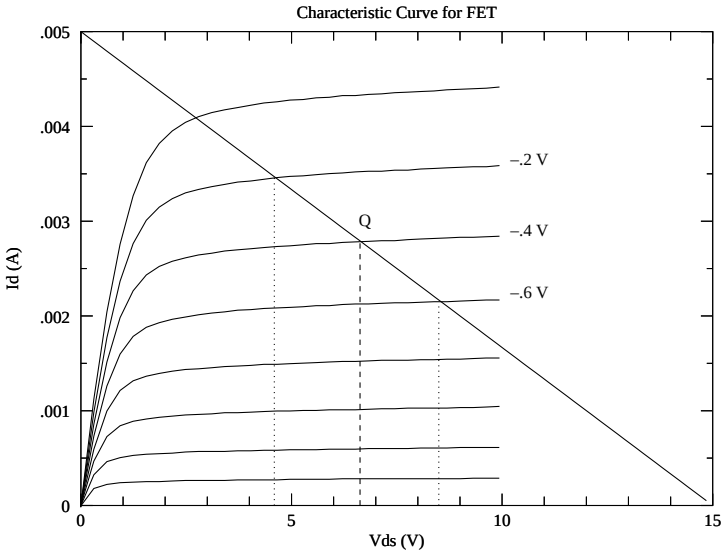
0. Load Lines and Characteristic Curves

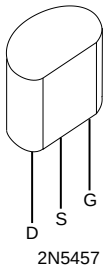
(See H&H Appendix F & G, web)

The characteristic curves for a FET along with the load line for the circuit of #2 are displayed below. *Report the value of R_D for this load line!* An operating point (a.k.a. quiescent point) Q has been selected at a gate bias voltage of $-.4$ V and drain current I_D of about 2.8 mA. The forward admittance y_{fs} (a.k.a. transconductance, g) at Q is given by:

$$y_{fs} = \frac{\partial I_D}{\partial V_G} \approx \left.\frac{\Delta I_D}{\Delta V_G}\right|_{V_{DS}=\text{const}} = \frac{2.8\text{ mA} - 2.1\text{ mA}}{-.4\text{ V} - -.6\text{ V}} = 3.5 \times 10^{-3}\Omega^{-1} \tag{1}$$

(In olden days the unit $\Omega^{-1} = \text{A/V}$ was be spelled "mho" and denoted: $\mho$ whereas the SI-unit folks would have you spell it "siemen" and denote as "S".) Note that if an inputted signal swings the gate voltage $\pm.2$ V, the source-to-drain voltage V_{DS} will range about 6.6 ± 2 V, i.e., we have a gain of 10. Note that use of larger R_D would force us to small I_D operating points and hence regions of lowered transconductance. (More closely spaced characteristic curves mean lowered g: explain please!) Smaller drain resistors have both more sharply sloped load lines (and hence smaller V_{DS} swings) and push us to operating points near the +15 V rail. We could maximize our gain if we had a flat load-line, e.g., a "resistor" that always drew 2.8 mA, independent of the voltage across it. Note that with such a flat load line through Q a swing in V_G of less than .1 V swings V_{DS} nearly rail-to-rail.





1. FET Characteristics

Select two different FETs of the same device number (e.g., 2N5457). Using the web-based[1] curve tracer, obtain characteristic curves for each. (Keep track of which characteristics correspond to which device.) Let's call the FET with the larger I_{DSS}: A; B is the other FET. Reading off the characteristic curve plot for FET A, make a table of I_D vs. V_G at, say, $V_{DS} = 7.5$ V. According to H&H Eq. (3.2), you should find:

$$I_D = k(V_G - V_T)^2$$

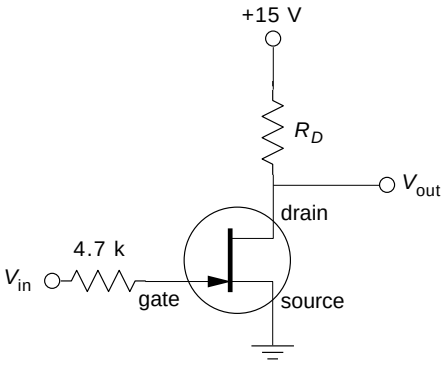
[1] `http://block.physics.csbsju.edu`

where V_T is the threshold voltage and k is determined by the FET's geometry, (These parameters will vary from device to device.) Fit (quadratic) and plot your data. Note by Eq. 1, that the slope of this relation is y_{fs}, a.k.a. g; calculate the derivative of your fit. Since the derivative of a quadratic is linear, g increases linearly for $V_G \in (V_T, 0^-)$. Calculate y_{fs} at $V_G = 0$. Use the fact that the slope should be zero when $V_G = V_T$ to calculate V_T from the fit's derivative. Compare your I_{DSS}, V_T ("cutoff voltage") and y_{fs} to the spec sheet values.

On your FET A characteristic curves, draw two tangent lines at $V_{\rm DS} = 0$: one using $V_G = 0$ V and the other using, say, $-.8$ V. Calculate two corresponding low-$V_{\rm DS}$ "resistances".

2. FET Voltage Amplifier

Construct the amplifier shown using FET A. Determine R_D by selecting a resistor that makes a "nice" load line on FET A's characteristic curves. Add the load line to your characteristic curves plot; select and label 'Q' your operating point. Use the dc offset of your function generator to bias the gate (with only a dc signal, initially) to your operating point. Measure the output voltage $V_{\rm out}$ as you change this dc bias $V_{\rm in}$. Plot the resulting points on your characteristic curves—they should lie near your load line. Now switch $V_{\rm in}$ to a sine wave (still with a dc offset). Again monitor $V_{\rm out}$ on your scope as you vary the dc bias, and record both the lower and upper levels of dc offset that result in distortion (rounded clipping) of $V_{\rm out}$. Return the bias level to an operating point near the center of the load line, keep the input amplitude small enough to avoid distortion, and measure the ac voltage gain $v_{\rm out}/v_{\rm in}$ where $v_{\rm out}$ is the ac part of $V_{\rm out}$ (e.g., peak-to-peak voltage) and $v_{\rm in}$ is the ac part of $V_{\rm in}$ at 10 kHz. Compare your result with the approximate theoretical value:



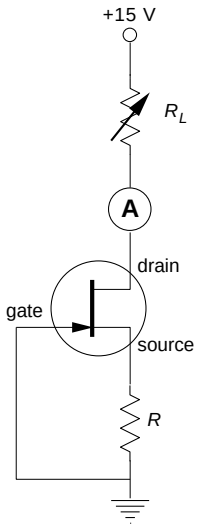
$$A_V = -gR_D$$

(Use the derivative of your part #1 fit to find g at your operating point.) Vary the input frequency (through several decades), and note that the gain is approximately constant throughout a large bandwidth. Find the high frequency $f_{-3\rm dB}$ where the gain is 3 dB less than 'usual'.

3. FET Current Source

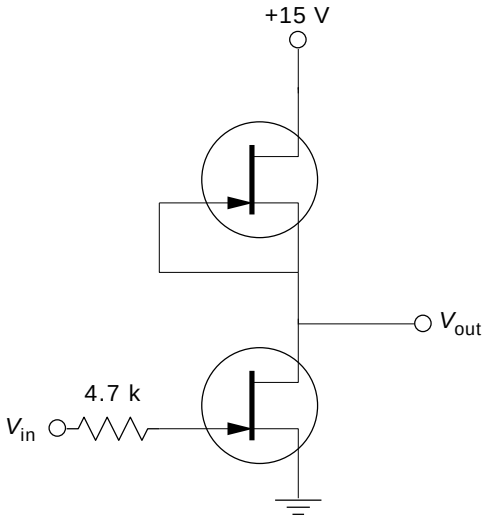
Construct the circuit shown using FET B. Use M-3800 as ammeter. Initially short gate and source (i.e., use $R = 0$). Measure the current with varying load R_L. Over what range of R_L is the current approximately constant (i.e., $\pm 10\%$)? How does this relate to the $V_G = 0$ characteristic curve (I_{DSS})?

Consider the case of a non-zero R. Using your characteristic curves, pick a "nice" value of I_D and the corresponding V_G. Calculate the required R and find a real R with approximately that value; build the circuit (record R actually used). How does the experimental "constant current" compare to the design value?



4. Active Load

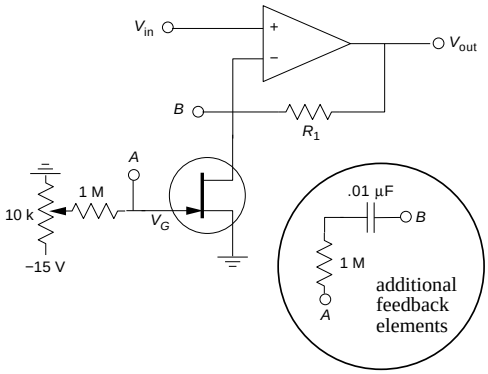
   In part #0 I noted that the best possible load for our amplifier was a constant current source. We've now constructed a FET constant current source using FET B; now make FET A use this constant current source (the gate-shorted-to-source version, as shown right) as its load. Find and report the gate bias voltage needed to maximize the small signal gain of this amplifier. Report that maximum gain.

   REMARK: Don't be overly impressed by the gain improvement of this new circuit. If we really want gain, for the price of two FETs we can get a 411 with a gain of 200,000. FETs are not gain superstars: use op-amps or bipolar transistors. FETs are masters of high input impedance. Perhaps I should have had you construct the actually useful active load voltage followers discussed in H&H 3.2.6, but followers never seem too impressive as lab projects.

5. Voltage-Controlled Gain Amplifier

   This circuit utilizes FET A as a "voltage-variable resistor" (VVR). The FET needs to be in the "ohmic region" where V_{DS} is "small" (e.g., smaller than the "gate drive": $V_G - V_T$). Explain why $V_{DS} = V_{\rm in}$ is expected. The aim is to construct an amplifier whose gain is controlled by a dc voltage on the FET's gate. Construct this circuit. (Find the 411 pinout in the previous lab.) Choose R_1 to be $\sim 40\times$ the $V_G = 0$ FET resistance found in #1. Drive the circuit with an ac signal (say, 5 kHz); use an amplitude small enough to avoid clipping (e.g., $V_{\rm in} < 100$ mV), and make a graph of gain A_V vs. pot-controlled, gate voltage V_G. You should recognize the op-amp circuit as a non-inverting amplifier... what is the equation for its gain? Where is the "second" resistor R_2? Looking at your FET characteristic curves what range of values does R_2 have? Operating at a fairly "large" negative control voltage (e.g., $V_T/2$), see how much you can increase the input signal amplitude before the output waveshape becomes distorted. Note the value of $V_{\rm DS}$ when this distortion sets in, and refer to your characteristic curves to explain its cause. This distortion should be lessened by adding the feedback elements shown between points A and B: try this fix and note its effect. (See p.161 of H&H for a quantitative explanation of this trick.) Save this circuit!

6. Automatic Gain Control (AGC)

The AGC circuit shown uses a voltage-controlled gain amplifier to keep V_{out} nearly constant over a wide range of amplitudes for V_{in}: such a device is useful in radios or tape recorders, for example, to maintain a constant-volume output despite an input signal whose strength may vary considerably. Build this circuit from the amplifier of part #5. Demonstrate your working circuit to your instructor! Measure the range of amplitudes for V_{in} over which V_{out} remains nearly constant in amplitude. Note that when the circuit is regulating the gain, the pot acts as the volume control. Below I've provided a duplicate copy of the circuit. Cut and tape this diagram into your lab book and then circle and label the following parts of the circuit: (1) a non-inverting op-amp with a voltage-controlled resistor, (2) a half-wave rectifier with capacitor filter, and (3) an integrator with summing inputs. Last year, a student commented: "if the inputs to the integrator are constant, the output will also be constant". Is this correct?

Explain qualitatively how this circuit works as a AGC amp. Begin by answering the following questions. In the previous part you saw that the gate voltage determined the gain. Which part of this circuit controls the gate voltage? What is required for the gate voltage to remain constant? What condition forces a decreasing gate voltage? Assume that V_{out} is too large, so the gain of the amplifier needs to be reduced. Report the chain of consequences that will cause the gate voltage to be correctly adjusted (up or down?) to bring about the required reduction in gain. If the pot is adjusted so that its voltage becomes more negative, report the chain of consequences that will affect (up or down?) the gain.