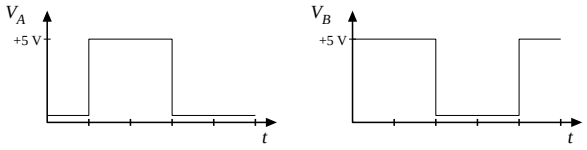
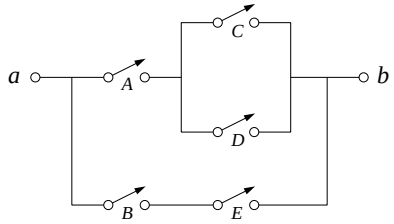
1. Answer the folowing questions on number systems. (Ref. HH 8.03)
   (a) Convert the following decimal numbers to binary: 28, 100, and 341
   (b) Convert the following sequence of decimal numbers to binary: 15, 16, 17, 18, 19
   (c) Convert the following binary numbers to decimal: 1101, 10101010, and 1111
   (d) Convert the above binary numbers to octal.
   (e) Convert the above binary numbers to hexadecimal
   (f) Convert 365_{10} to BCD
   (g) Convert the BCD number 0100,0001 to binary.

2. Without converting to decimal, directly add the following binary numbers. Then check your answers by converting each number to decimal.
   (a) $111011 + 101110$
   (b) $01011 + 110$
   (c) $010101 + 01101$

3. Voltages V_A and V_B (plotted below left as functions of time) are used as inputs to simple gates. Graph the gate output as a function of time if the gate is:
   (a) AND (i.e., $V_A \cdot V_B$)
   (b) OR (i.e., $V_A + V_B$)

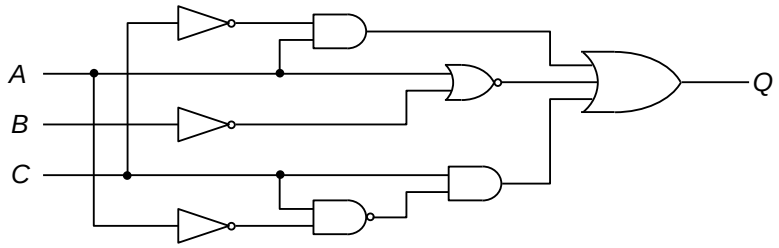
   You have probably answered this question assuming positive-true (HH p. 472 + 8.07) logic. Answer again assuming negative-true logic.





4. Consider the switch network shown above right. Deduce the Boolean expression for the condition that the circuit conducts current between a and b. (A closed switch is to be consider true.)

5. Consider the below mess of gates:



   (a) Convert the mess of gates into the equivalent boolean expression.
   (b) Use boolean algebra to reduce your boolean expression.
   (c) Express your reduced expression in gates.
   (d) Draw this circuit and label the logic level of every wire assuming $(A, B, C) = (0, 0, 0)$.

6. The statement "A or B and C" can be interpreted in two ways. Write unambiguous Boolean expressions for each interpretation and express the resulting expression in a circuit of simple gates.

7. Go to the Texas Instruments web site (`www.ti.com`) and find the data sheet for a 7400 (quad NAND gate). Print out the first page (which should show the pinouts for the various packages). Go to the Digi-Key web site (`www.digikey.com`) and find the part number and price for a 7400 in the 14 pin DIP package.

8. Consider the diode-logic circuit with inputs A, B and C shown below left.

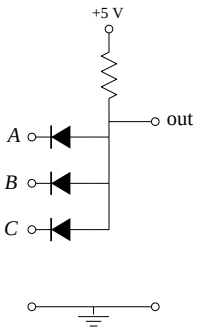
   (a) Suppose C is brought low by connecting it to ground, while A and B unconnected. What is the output voltage?

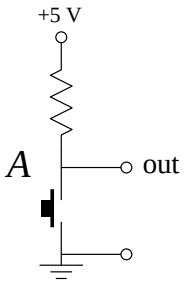
   (b) Suppose C is brought low by connecting it to ground, while A and B remain connected to +5 V. What is the output voltage?

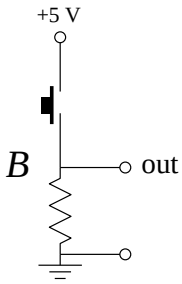
   (c) Suppose both B and C are held low by connecting it to ground, while A is connected to +5 V. What is the output voltage?

   (d) What logic function is implemented by this circuit?

   (e) Suppose C is brought low by connecting it through a 1 kΩ resistor to ground, while A and B remain connected to +5 V. What is the output voltage?







9. Consider two possible designs for a push-button controlled logic level as diagrammed above right. In design A, a NO SPST push button (HH p. 54) is connected to +5 V via a resistor ('pull-up resistor'). In design B, a NO SPST push button is connected ground via a resistor ('pull-down resistor'). What problems result (in each case) if R is made too-large? What is a proper choice for R (approximately for each case)? Generally speaking which design is superior for TTL gates? Report why.

10. Design a majority-rule voting system for a committee of three members. Each member is provided with a yes/no switch; the output is true if and only if the vote passes. Your design should include both a circuit of simple gates implementing the function and the corresponding Boolean expressions.

11. (a) Show that $A + \overline{A}B = A + B$ using two of the following three methods: Venn Diagram, complete enumeration of all cases in a truth table, or by Boolean algebra.

    (b) Show:

$$\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + AB\overline{C} + ABC = \overline{A \cdot \overline{B}}$$

    (c) Directly implement each side of this expression in gates. How many gates are saved by using the reduced form?

12. (a) Consider

$$T = (A + B)(\overline{B} + A)$$

    Draw the gate circuit that follows directly from this statement.

    (b) Assume $A = 1$ and $B = 0$. Directly on your circuit diagram, label the logic level of each wire.

    (c) Reduce the Boolean expression for T. Show that your reduced expression in fact produces the same output as the full expression with the inputs $A = 1$ and $B = 0$.

13. Reduce the following expressions:

    (a) $\overline{A} \cdot \overline{((B \cdot C) + B)} \cdot \overline{A}$

    (b) $\overline{A}\,\overline{B} + (A + \overline{B})$

    (c) $(A + AB) + \overline{A}B$

    (d) $(\overline{A} + \overline{B})(A \cdot \overline{B})$

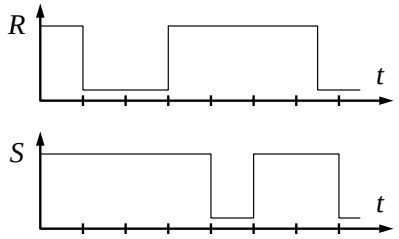
    (e) $[(AB + A\overline{B}) + AB] + \overline{A}B$

14. (a) Write the sum-of-products (minterm) expression for this truth table.

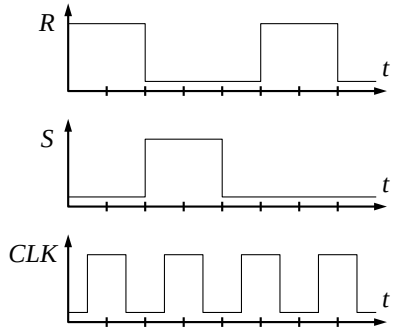
    (b) Write the product-of-sums (maxterm) expression for this truth table.

A	B	C	T
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

15. Consider the cross-NAND SR FF with S, R inputs (plotted as a function of time) as shown below. Graph Q (along with R, S) as functions of time. (The graphs for this and the following problems should be 'stacked', as in the below examples, so that the simultaneous behavior of all the signals can be assessed.) HH Fig. 8.47 is a cross-NAND SR FF, but 'bubble pushing' has moved the invert to the inputs with AND→OR.



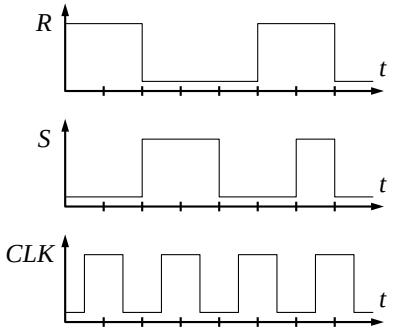
16. Consider the level-triggered cross-NAND SR FF (HH Fig. 8.51) with S, R, CLK inputs (plotted as a function of time) as shown below. Graph Q (along with R, S, CLK) as functions of time.



17. Consider the edge-triggered cross-NAND SR FF (action on high S & R) with S, R, CLK inputs (plotted as a function of time) as shown below. Graph Q (along with R, S, CLK) as functions of time for:

    (a) positive edge triggered SR FF

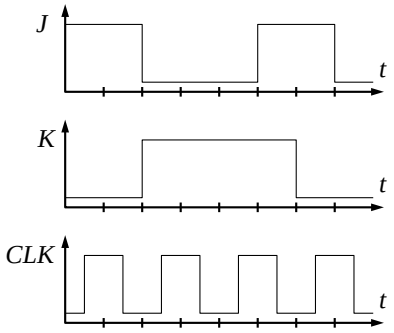
    (b) negative edge triggered SR FF



18. Consider the edge-triggered JK FF (HH p. 509) with J, K, CLK inputs (plotted as a function of time) as shown below. Assume that initially $Q = 0$. Graph Q (along with J, K, CLK) as functions of time for:

    (a) positive edge triggered JK FF

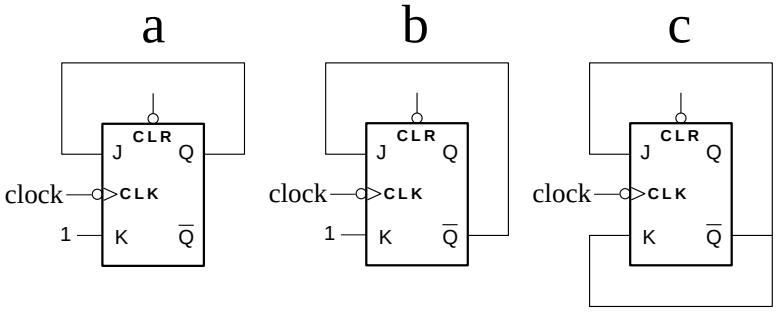
    (b) negative edge triggered JK FF



19. A new type of controlled flip-flop satisfying the below state table is required for a design. Show how you can make this FF from a JKFF an a few simple gates.

A	B	Q_{n+1}
0	0	$\overline{Q}_n$
1	0	Q_n
0	1	0
1	1	1

20. For each of the following circuits, assume that initially $Q = 0$ and then a series of clock pulses are applied to CLK. For each circuit plot Q and CLK as functions of time.



21. (a) A simple indicator of minimum overnight temperature is desired. Assume that three normally open SPST switches are available that close when the temperature falls below 10° C, 5° C, and 0° C. (The switches open again when the temperature rises above the set point.) Design an instrument with three light indicators; each indicator lights and holds if the temperature falls below its set point. A reset button should be provided so that the instrument can be cleared after reading it the following morning. Assume that the indicator lights operate using the usual logic level voltages (HIGH=light on, LOW=light off).

    (b) In a conventional mercury thermometer a column of mercury moves up or down responding to the current temperature. Design a instrument in which a column of lighted lights acts like the mercury column: additional lights lighting (lengthening the lighted column) as the temperature rises. Assume that 30 switches are available with set points in increments of 1° C (i.e., 0° C, 1° C, 2° C, ..., 29° C).

22. A building has a turnstile for incoming people and another turnstile for people leaving the building. The output of a turnstile is generally HIGH but, when a person passes through it, a short ($\sim$ 100 ns) LOW pulse is produced. Show how, with a just a handful of extra gates, a 74191 can be used to display the number of people actually in the building. Note: the 74193 counter which exactly solves this problem: a counter with separate up and down clock inputs, but you are instead to use the '191 described used in Lab 3. The first thing you must do is combine the two turnstile outputs to make one clock—you may assume that the pulses are so short that they *never* overlap. Next you need to figure out how to control the '191's $\overline{U}/D$ pin.

23. A crossed-NAND SR FF has an active low Set pin ($S \to 0 \Rightarrow Q \to 1$) and an active low Reset (clear) pin ($R \to 0 \Rightarrow Q \to 0$). The setting and clearing action is immediate: there is no clock. A D FF has a Data pin (D), the value of which is read and transferred to the output when the Load pin (L) goes high. Consider the process of making a D FF from a SR FF and some additional gates. The Load and Data lines must somehow control the Set and Reset pins to make the SR FF act as desired.

    (a) Begin by thinking what S and R need to be for all possible combinations of D and L. This is best done by completing the truth tables:

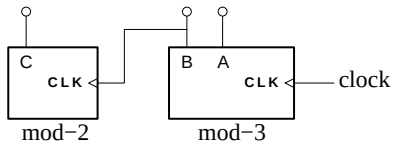
D	L	S
0	0	
1	0	
0	1	
1	1	

D	L	R
0	0	
1	0	
0	1	
1	1	

    (b) Write down the Boolean expression for each truth table.

    (c) Draw the circuit required for D and L to drive R and S.

24. A mod-3 counter (e.g., HH Fig. 8.60 p. 514 with output digits BA) and a mod-2 counter (e.g., a toggling FF with output digit C) are connected together as shown below. Graph the C, B, A outputs for a square wave clock input. Show that C is a symmetrical square wave with a frequency 1/6 of the input frequency. Assume that both counters are synchronous, but with an output delay of 30 ns. What cycle of C, B, A states is actually produced by this asynchronous connection?



25. An elevator services three floors of a hotel. There are three logical variables: E_1, E_2, E_3, which record the floor at which the elevator sits. $E_i = 1$ if the elevator is on the i^{th} floor and is 0 otherwise. (For example, if the elevator is on the 2^{nd} floor, $E_2 = 1$ while $E_1 = E_3 = 0$. Assume exactly one of the E_i will be 1.) On each floor there is an elevator call button. The logical variables C_1, C_2, C_3 record unsatisfied requests for elevator service. $C_i = 1$ if the elevator is requested on the i^{th} and is 0 otherwise. (For example, if $C_2 = 0$ while $C_1 = C_3 = 1$, the elevator is requested on the first and third floors.) In responding to call requests the elevator can go up (if up-motor control U=1) or down (if down-motor control D=1) or not move (if U=0 and D=0). (U=1 and D=1 should never occur.) Write a logical expression for U as a function of inputs E_i and C_i. Do the same for D. Your answer should represent rational elevator behavior; for example the elevator must answer the *closest* call request.

26. The logic circuit for a 7490 (shown below) involves negative edge triggered JK FF and RS FF. Each of the FF has asynchronous (direct) set (S_D) and re-set (clear) (R_D) inputs.

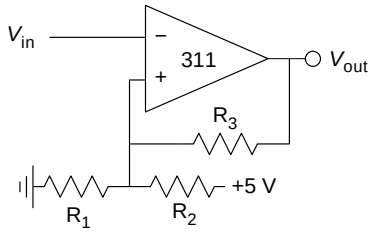
    (a) Graph the important signals as a function of time to show that Q_1, Q_2, Q_3 and C_{p1} form a Mod-3 counter.

    (b) What is the output if MS_1 and MS_2 are both HIGH?

    (c) If Q_0 is connected to C_{p1} and the device is clocked on C_{p0}, what output result? Explain and graph the output of the important signals.

    (d) If Q_3 is connected to C_{p0} and the device is clocked on C_{p1}, what output result? Explain and graph the output of the important signals.

27. Consider the classic Schmitt[1] trigger circuit, where you can assume that the output of the 311 swings between +5 V and 0 V. (This need not actually be the case; for example, the 311 would require a pull-up resistor.) Design a circuit which has transitions at +1.0 V and +1.5 V. As you recall, when the 311's output is low we have a voltage divider with $R_1 \parallel R_3$ and R_2 whereas when the 311's output is high we have a voltage divider with R_1 and $R_2 \parallel R_3$. The difference between these two, ΔV, is given by a voltage divider with $R_1 \parallel R_2$ and R_3.



The above question has some difficulties. First it requests three answers (R_1, R_2, R_3) from two equations (the two set-point voltages). Systems of equations with more unknowns than equations cannot in general be solved. (They are called underdetermined.) While mathematicians may not approve of such problems, they occur all the time in real life. They are what "design" is all about: options to be selected. In this question if (R_1, R_2, R_3) is a solution then so is (xR_1, xR_2, xR_3), for any multiplier x. Design here then amounts to setting an overall scale for the resistors. "Reasonable"[2] resistor values are often in the range kΩ to MΩ. Furthermore, actual for-sale resistors come in a limited range of values (see HH p. 1053). A second problem has to do with the non-linear nature of the equations for the set-point voltages. A practical ('trial and error') way of solving these equations is to find the $R_3/(R_1 \parallel R_2)$ that produces the the desired level of hysteresis (ΔV) and then use the simple voltage divider equation (for a voltage in the suggested range) to relate R_2 and $R_1 \parallel R_2$. Once the R_i have been found you can use the exact equations to determine the actual switching points. This results in fairly simple algebra, and usually works adequately (if not just iterate the process). *Mathematica*, of course, can provide an immediate exact solution...

```
Solve[{1.5/5==r1/(r2 r3/(r2+r3)+r1), 1./5==r1 r3/(r1+r3)/(r1 r3/(r1+r3)+r2)},{r1,r2}]
```

    (a) Make a design using *Mathematica*.

    (b) Made a design using the approximate approach.

[1] Otto Herbert Schmitt 1923–1998; Ph. D. 1937 Washington University (St. Louis) (physics, zoology), UMn Bio-Physics prof 1941–98

[2] "Small" resistors may lead to large power loss: V^2/R; "large" resistors are more susceptible to noise and stray capacitance problems.

28. For this problem you will need the pinout and function table of the '121 monostable. The required information can be found in Fig. 8.64 HH p. 518 and/or `sn74121.pdf` (downloaded from `ti.com` and placed in the class web site). Design circuits (and record exact wiring diagrams) that do the following:

    (a) make a 20 μs pulse on a positive edge

    (b) make a 20 μs pulse delayed by 1 ms from a negative edge

    (c) make a 50 kHz symmetrical square wave

29. Refer to the 74121 pinout function table described in the previous problem and answer the following multiple choice questions:

    (a) If A_1 and B are high, the monostable will produce a pulse if:

        A. A_2 goes low to high

        B. A_2 goes high to low

        C. neither as it is inhibited

    (b) If A_1 is low and B is high, the monostable will produce a pulse if:

        A. A_2 goes low to high

        B. A_2 goes high to low

        C. neither as it is inhibited

    (c) If A_1 and B are low, the monostable will produce a pulse if:

        A. A_2 goes low to high

        B. A_2 goes high to low

        C. neither as it is inhibited

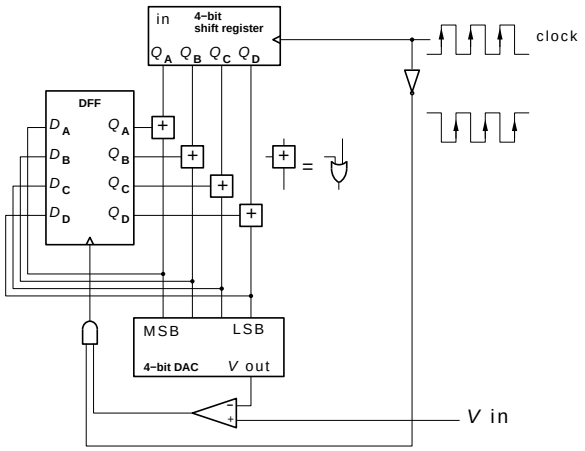
    (d) If A_1 is low and the voltage on A_2 is unknown, the monostable will produce a pulse if:

        A. B goes low to high

        B. B goes high to low

        C. it depends on the voltage on A_2

30. Consider a cartoon version of a 4-bit successive approximation ADC:



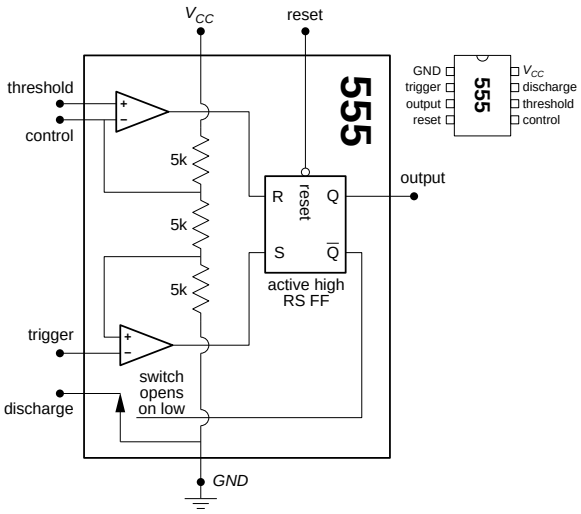
    Assume that controls not shown on the diagram arrange that at the start of a conversion the DFF and shift register are cleared and then one 1, starting in Q_A, shifts to the right through the shift register. Assume the DAC is perfectly linear, producing $V_{\text{out}} = \frac{1}{3}$ digital in, i.e., +5 V out for an input of $15 = 1111_2$ (and 0 V out for input of 0). Graph the DAC output during the conversion if $V_{\text{in}} = 3.14$ V. Graph the DAC output during the conversion if $V_{\text{in}} = 2.99$ V. What is the smallest V_{in} that results in a digital output of 1? Carefully compare the ideal ADC curve (HH Fig. 9.44A, p. 615) to what would result with this ADC. What is the difference?

31. Assume that the cost of a flash ADC is proportional to the number of comparators and that the conversion time of a successive approximation ADC is proportional to the number of bits. Compare the costs of a 7-bit flash ADC and an 8-bit flash ADC. Compare the conversion times of a 7-bit successive approximation ADC and an 8-bit successive approximation ADC.

32. Consider the diagram of a 555 (or the equivalent diagrams: HH Fig. 5.32).

    (a) Draw the circuit that produces continuous oscillation from the 555. Describe (words!) how the circuit works.

    (b) Draw the circuit that allows the 555 to act as a one-shot (monostable). Describe (words!) how the circuit works.



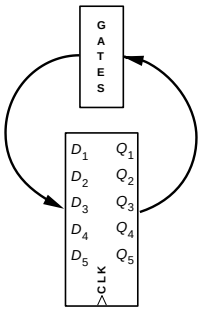
33. We return here to the problem of finding circuits for state diagrams. Recall that the current state must totally control the following state. But what if we want various futures for a state in various circumstances?

    The Morse Code is a bit unusual encoding of letters in that the letters require differing numbers of dot/dashes from one (E=dot=0, T=dash=1) to four (e.g., Q=dash-dash-dot-dash). If we restrict ourselves to the eight letters expressed with 3 bit Morse Code expressions: (D=100, G=110, K=101, O=111, R=010, S=000, U=001, W=011), we can make some odd sentences like: DORKS GROK SORROW. Imagine a circuit that cycles through these letters (i.e., D→O→R→K→S→ etc.). However see that the four Os have different targets: O→R, O→K, O→W. Therefore the *circuit* must distinguish four different types of O (but of course the display will show the same lettershape for each O state). Thus:

    $\mathrm{D} \to \mathrm{O}_0 \to \mathrm{R}_0 \to \mathrm{K}_0 \to \mathrm{S}_0 \to \mathrm{G} \to \mathrm{R}_1 \to \mathrm{O}_1 \to \mathrm{K}_1 \to \mathrm{S}_1 \to \mathrm{O}_2 \to \mathrm{R}_2 \to \mathrm{R}_3 \to \mathrm{O}_3 \to \mathrm{W}$

    Each state will now be labeled with five bits $Q_1Q_2Q_3Q_4Q_5$ — $Q_3Q_4Q_5$ specifying the lettershape and Q_1Q_2 distinguishing the various 'identical' letters. Fill in the below table so it displays the desired cycle and the D_i required to generate it. Find a boolean expression for one of the D_i in terms of the Q_i.

Q_1	Q_2	Q_3	Q_4	Q_5	D_1	D_2	D_3	D_4	D_5
0	0	1	0	0					



34. HH describes more than half a dozen temperature transducers. Pick out three of these and 'compare and contrast' them—that is report their advantages and disadvantages. Describe a situation in a physics lab requiring a temperature measurement and report which transducer you would select and why.

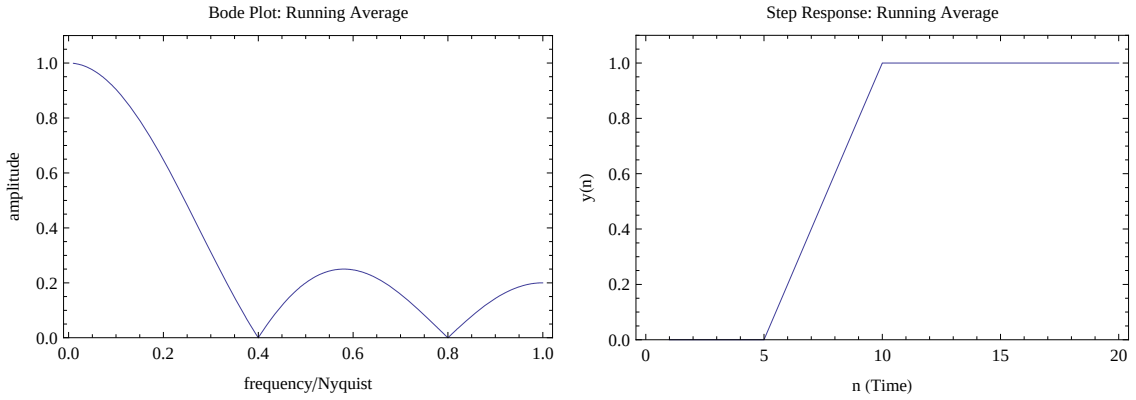
35. A running average (of five) digital filter would be described by the equation:

$$y_n = \frac{1}{5}\ (x_n + x_{n-1} + x_{n-2} + x_{n-3} + x_{n-4})$$

Let x_n be a unit step that occurs at $n = 6$, i.e.,

$$x_n = \begin{cases} 0 & n < 6 \\ 1 & n \geq 6 \end{cases} \qquad \text{where you are to assume: } y_n = 0 \text{ for } n < 6$$

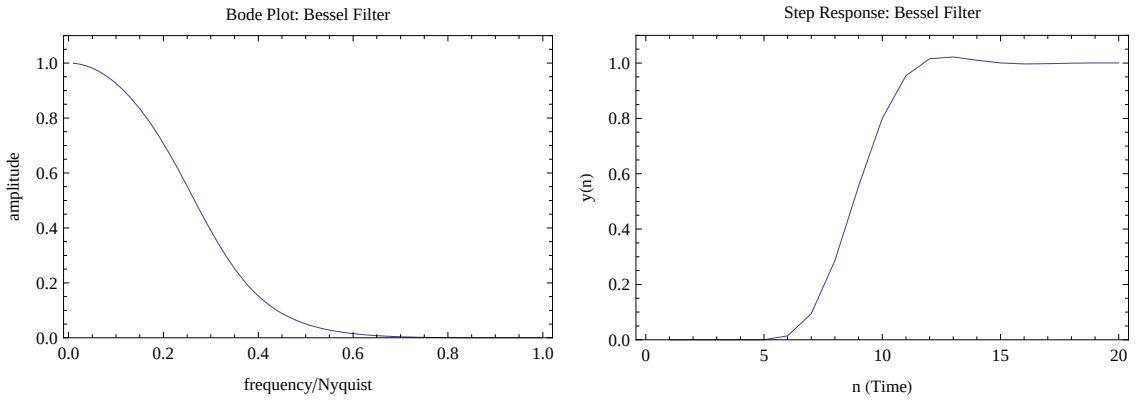
The below right shows the resulting response (y_n) to this unit step input. The below left shows a Bode plot: the equilibrium y_n amplitude when the input x_n is a unit-amplitude sinusoid with frequency f. (The x axis is f divided by the Nyquist frequency.)



A fourth order Bessel digital filter would be described by the equation:

$$y_n = \frac{1}{68.94}\ (x_n + 4x_{n-1} + 6x_{n-2} + 4x_{n-3} + x_{n-4}) - 0.05034y_{n-4} + 0.3599y_{n-3} - 1.0459y_{n-2} + 1.5042y_{n-1}$$

The below right shows the resulting response (y_n) to the unit step input. The below left shows a Bode plot: the equilibrium y_n amplitude when the input x_n is a unit-amplitude sinusoid with frequency f. (The x axis is f divided by the Nyquist frequency.)



(a) Calculate y_7 for both filters.

(b) If the sampling rate is 10000 Hz, what is the Nyquist frequency?

(c) If the input is a unit-amplitude sinusoid with frequency $f = 2500$ Hz, use the above graphs to find the resulting y amplitude for both filters.

A. CMOS, TTL
B. DIP
C. VLSI
D. Tri-state (Hi-Z)
E. pull-up resistor
F. logic probe
G. gate delay
H. glitch
I. fan-out
J. wired OR
K. two's complement
L. decoder
M. encoder
N. multiplexer (MUX)
O. demultiplexer (deMUX)
P. RSFF
Q. JKFF
R. DFF
S. synchronous
T. ripple counter
U. shift register
V. maxterm (POS), minterm (SOP)
W. Bus
X. state diagram
Y. PLA or PAL
Z. FPGA

a. ROM, PROM, EPROM
b. RAM (D & S)
c. address
d. register
e. stack
f. stack pointer
g. program counter
h. BCD
i. ASCII
j. baud
k. byte, nibble
l. comparator
m. Schmitt trigger
n. hysteresis
o. monostable
p. VCO
q. transducer
r. DAC
s. dual-slope ADC
t. successive approximation ADC
u. flash ADC
v. DSP
w. FFT
x. Bode plot
y. Nyquist frequency
z. FIR & IIR digital filters

Dr. Adam Whitten designed the following prolbmes

37. Reduce the following boolean expressions:

    (a) $(A + \overline{B})(A + B)$

    (b) $(A + B)(\overline{A}B)$

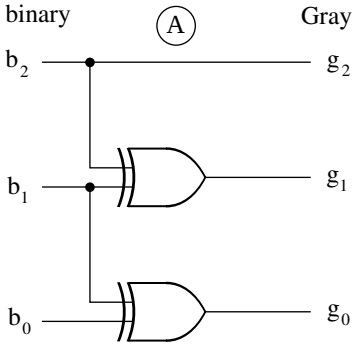
    (c) $\overline{AB}A\overline{B}$

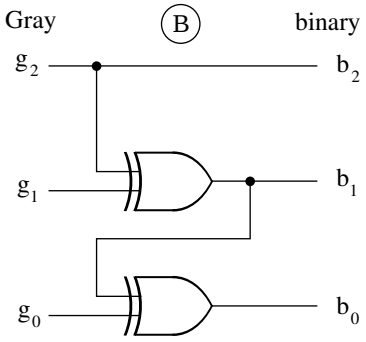
    (d) $\overline{\overline{A} \cdot (\overline{A} + \overline{B}) \cdot (A + \overline{B})}$

    (e) $AB + \overline{A}\,\overline{B} + A\overline{B} + \overline{A}B$

    (f) $\overline{(A + B)(A + C) + A(B + C)}$

38. The figure to the below shows circuits for converting a 3-bit binary number to Gray code (A) and a 3-bit Gray code to binary (B). Show by means of a truth table that the circuits behave as indicated.





39. Given the truth table at the right:

    (a) Write out the sum of products (SOP).

    (b) Minimize the expression using boolean algebra.

    (c) Make a Karnaugh map and write out the sum of products. Is it the same as your minimized expression from part (b)? If not, explain why (hint: look in your Karnaugh map).

    (d) Apply logic identities to your SOP expression from (c) to generate a product of sums (POS).

    (e) Draw circuit diagrams for the expressions in (c) and (d).

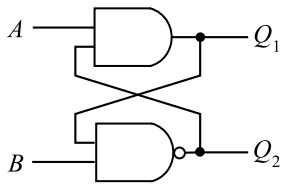
    (f) Download the 74LS54 AND-OR-INVERT datasheet from `www.datasheetcatalog.com` and draw out how you would implement this circuit using this AOI chip and one hex inverter chip. Draw the AOI chip as a rectangle with the pins clearly labeled.

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

40. Draw out how to implement the truth table in problem 39 using a 74151 8-input multiplexer. Draw a block diagram of the multiplexer and clearly indicate how each pin is connected. Either download the 74151 datasheet or see Horowitz and Hill page 495.

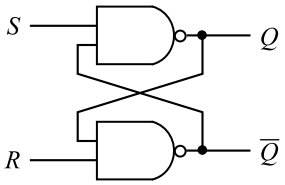
41. Design a temperature warning circuit for a cluster of four temperature sensors *using a single chip*. The output of a temperature sensor goes high when a temperature threshold is reached. The circuit should output a logic high when 3 of the 4 sensors are high.

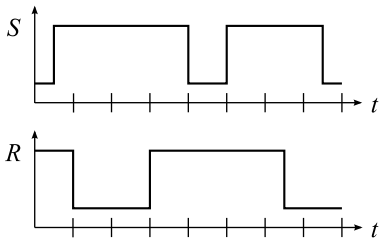
42. Complete the truth table for the non-standard flip-flop circuit below. Make sure to indicate any undetermined conditions.



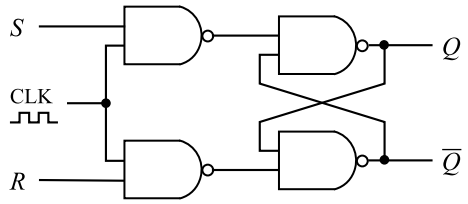
A	B	Q_1	Q_2
0	0		
0	1		
1	0		
1	1		

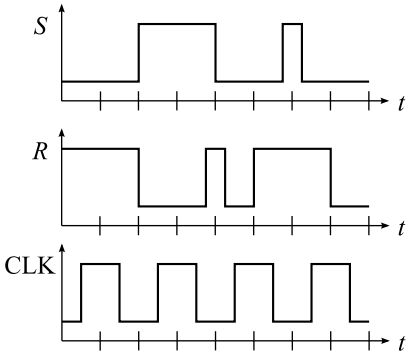
43. For the cross-NAND SR FF shown below, graph Q and $\overline{Q}$ as functions of time for the given S and R inputs at the right. Stack the graphs of S, R, Q, and $\overline{Q}$ so the simultaneous behavior of the inputs and output can be examined.





44. For the clocked level-triggered cross-NAND SR FF shown below, graph Q and $\overline{Q}$ as functions of time for the given S, R, and CLK inputs at the right. Stack the graphs of S, R, CLK, Q, and $\overline{Q}$ so the circuit behavior can be examined.

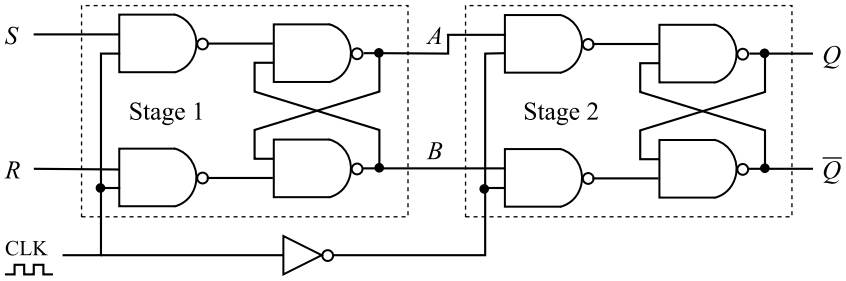


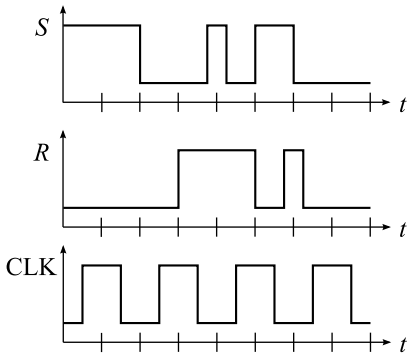


45. The circuit below contains two stages, each of which is a clocked level-triggered SR FF. The clock is inverted before going to Stage 2, requiring a complete clock pulse before the output changes. Note: Some texts erroneously call this an "negative edge-triggered" SR FF.

    (a) Show that the output changes at the negative clock edge according to the values of S and R by stacking graphs of S, R, CLK, A, B, $\overline{\text{CLK}}$, and Q for the given inputs.

    (b) What modification would turn this into a clocked "positive edge-triggered" SR FF?



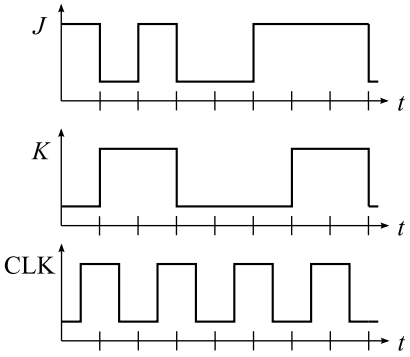


46. Consider an edge-triggered JK FF. Graph the output Q as a function of time by stacking graphs of J, K, CLK, and Q for the given inputs for:

    (a) a positive edge-triggered JK FF

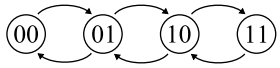
    (b) a negative edge-triggered JK FF

    Place both (a) and (b) in the same stacked graph to help show the differences between the two. Make sure to clearly label (a) and (b).



47. Design a circuit using edge-triggered JK FFs whose outputs $Q_2Q_1Q_0$ count from 000 through 111 and then start over again. Note: You will build this circuit in lab number 2.

48. Design a circuit using edge-triggered JK FFs that will follow the state diagram shown to the right. Hint: the next state depends on the current value and whether the count is increasing or decreasing. "Increasing" or "decreasing" is considered a state and you can use a FF to indicate this state.



49. Using the 74121 datasheet, design circuits to perform the following functions. Draw your circuits clearly and record the values of any external capacitors and resistors used.

    (a) Generate a 50 μs pulse on a positive edge

    (b) Generate a 50 μs pulse delayed by 1 ms from a negative edge

    (c) Generate a 50 kHz symmetrical square wave

50. Explain why thermistors are preferred over thermocouples for controlling the temperature of an environment.

51. Explain the differences between a photodiode and a phototransistor.

52. Digital filters are used in digital signal processing. The theory is outlined at `http://en.wikipedia.org/wiki/Digital_filter` and relies on Z-transforms (related to Laplace transforms). The details are complex, but recognize that the transfer function represents the amplitude of the output divided by the amplitude of the input.

    Finite impulse response (FIR) filters depend only on the sampled input (see `http://en.wikipedia.org/wiki/Finite_impulse_response`) while infinite impulse response (IIR) filters depend on both the sampled input and the sampled output (see `http://en.wikipedia.org/wiki/Infinite_impulse_response`).

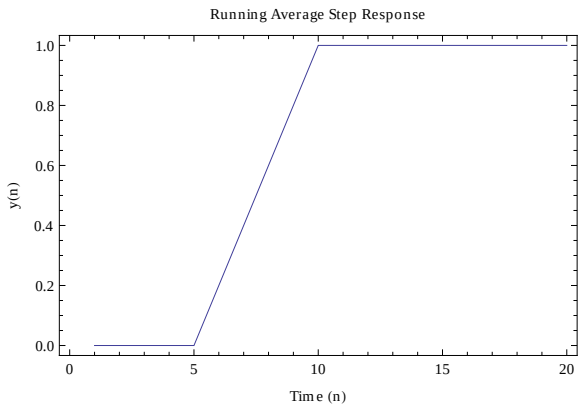
    A digital filter made from a running average of five samples is an example of a FIR filter and is described by the equation:

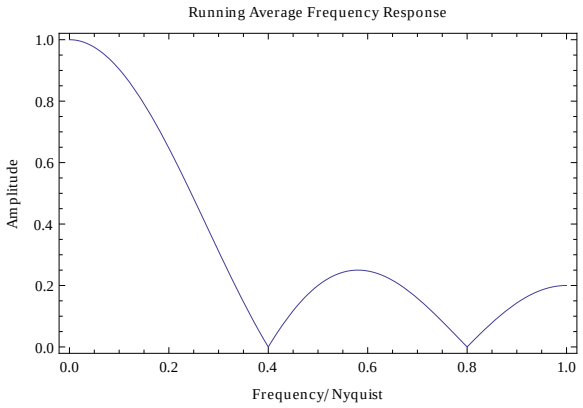
$$y_n = \frac{1}{5}\left(x_n + x_{n-1} + x_{n-2} + x_{n-3} + x_{n-4}\right)$$

    Consider the input, x_n, to be a unit step that occurs at $n = 6$

$$x_n = \begin{cases} 0 & n < 6 \\ 1 & n \geq 6 \end{cases} \qquad \text{where it is assumed that } y_n = 0 \text{ for } n < 6$$

    The following graphs show the response to a step input and a sine wave input. The left graph shows the resulting response, y_n, to the unit step input in the time domain. The right graph shows the frequency response: the equilibrium y_n amplitude (normalized to 1) when the input x_n is a unit amplitude sine wave. The x-axis is f divided by the Nyquist frequency.

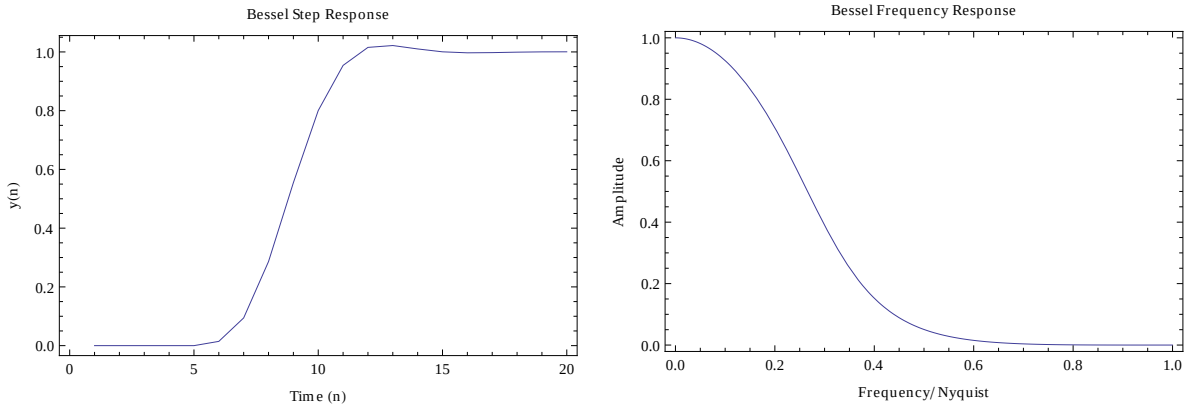




A 4^{th} order low pass Bessel digital filter is an example of an IIR filter and is described by the equation:

$$\begin{aligned} y_n &= \frac{1}{68.94}(x_n + 4x_{n-1} + 6x_{n-2} + 4x_{n-3} + x_{n-4} \\ &\quad -0.0503y_{n-4} + 0.3599y_{n-3} - 1.0459y_{n-2} + 1.5042y_{n-1}) \end{aligned}$$

The following graphs show the response to a step input and a sine wave input. The left graph shows the resulting response, y_n, to the unit step input in the time domain. The right graph shows the frequency response: the equilibrium y_n amplitude (normalized to 1) when the input x_n is a unit amplitude sine wave. The x-axis is f divided by the Nyquist frequency.



(a) Calculate y_7 for both the running average filter and the Bessel filter.

(b) If the sampling rate is 10000 Hz, what is the Nyquist frequency?

(c) If the input is a unit amplitude sine wave with frequency $f = 2.5$ kHz, use the graphs to approximate the resulting y amplitude for both filters.

(a) Calculate y_7 for both the running average filter and the Bessel filter.

(b) If the sampling rate is 10000 Hz, what is the Nyquist frequency?

(c) If the input is a unit amplitude sine wave with frequency $f = 2.5$ kHz, use the graphs to approximate the resulting y amplitude for both filters.

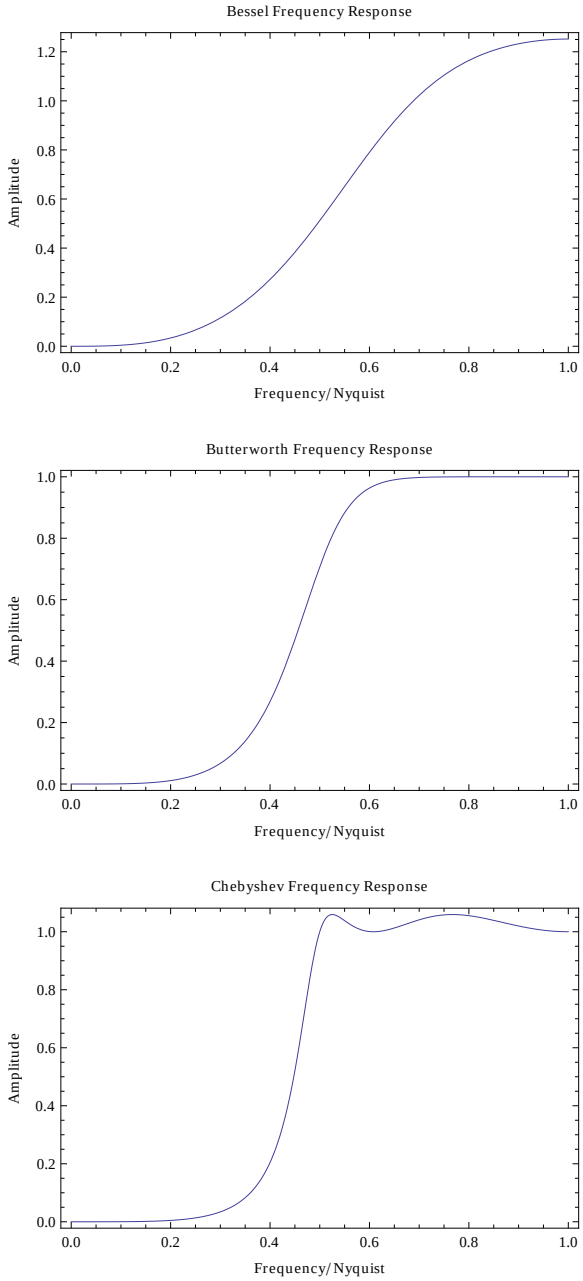
53. The graphs to the right show frequency response plots for three 4^{th} order high pass filters — Bessel, Butterworth, and Chebyshev.

All three filters have a corner frequency of 2500 Hz and are designed for a sampling rate of 10000 Hz. The Chebyshev filter has the ripple specified as -0.5 dB.

(a) What is the Nyquist frequency for the three filters.

(b) Use the graphs to estimate the output amplitude for a unit amplitude sine wave input with a frequency of 2500 Hz.

(c) Describe in words the differences between the three filter responses.



54. The Mathematica code in DSP.filter.txt displays the behavior for a 5^{th} order Butterworth filter (sampling rate = 10000 Hz, corner frequency = 1000 Hz) using the recursion relation found from `http://www-users.cs.york.ac.uk/~fisher/mkfilter/`. Use this website to design your own filter $\Longrightarrow$ you choose the parameters, but make sure to include them with your homework. Use Mathematica code similar to that in DSP.filter.txt to display the properties of your filter. Add comments to the code to explain what it is doing and print it out. Make plots of (a) response to a step, (b) response to a passed frequency, (c) response to a blocked frequency, and (d) the frequency response.