Bipolar Junction Transistors

0. (a) **Load Lines and Characteristic Curves**

The below figure shows the characteristic curves for a BJT along with the load line for the simple common emitter amplifier (similar to circuit of #4, but with $R_E = 0$). *Report the resistance R_C and supply voltage, V_{CC}, implied by this load line.* We focus on the operating point Q appropriate for a base current $I_B = 0.03$ mA. Note that the collector current I_C at the operating point is about 3.2 mA. Recall that the current gain (a.k.a., forward transfer current ratio) $\beta = h_{fe}$ where:

$$h_{fe} = \frac{\partial I_C}{\partial I_B} \approx \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{const}} = \frac{3.2\text{ mA} - 2.0\text{ mA}}{0.03\text{ mA} - 0.02\text{ mA}} = 120$$

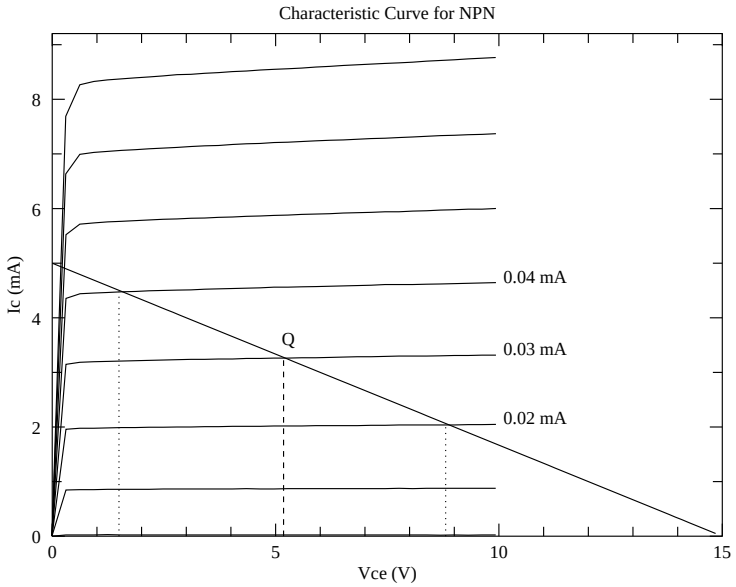
If an inputted signal swings the base current ± 0.01 mA, the collector-to-emitter voltage V_{CE} will range about 5.2 ∓ 3.5 V. While the current gain is known to be $\beta = 120$, the voltage gain depends on the input impedance, i.e., we need to know what input voltage swing is required to swing the base current by 0.01 mA. The base-emitter resistance depends on the collector current. H&H (p.92) says:

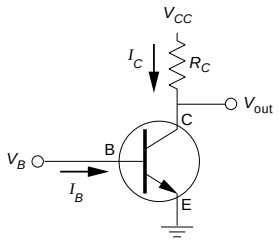
$$r_e = \frac{(kT/q)}{I_C} \approx \frac{25\text{mV}}{I_C} = \frac{25\Omega \cdot \text{mA}}{I_C}$$

For this operating point $I_C = 3.2$ mA, so $r_e = 7.8\ \Omega$. The input impedance is then approximately $h_{ie} = \beta r_e = 940\ \Omega$. So:

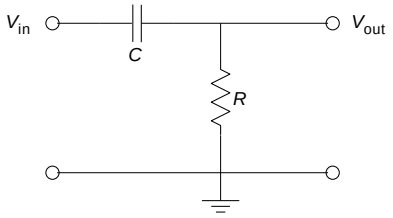
$$\Delta V_{\text{out}} = -\Delta I_C R_C = -\beta \Delta I_B R_C = -\frac{\beta R_C}{\beta r_e}\,\Delta V_B = -\frac{R_C}{r_e}\,\Delta V_B$$

The calculated voltage gain is nearly 400! As spelled out in H&H (p.94) you should never be enticed by this large gain, instead use the "emitter degeneration" circuit described in #4.





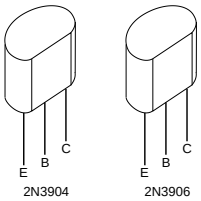
(b) **Biasing & Blocking Capacitors**



The above circuit requires a base current of 0.03 mA to set the operating point Q. Thus some "biasing resistors" are needed to set up this quiescent state. As a result in normal operation the base will sit about .6 V above ground. Similarly the output voltage was offset about 5.2 V above ground. Thus to get signals into and out of our amplifier we must use *blocking capacitors* to block the dc offsets while allowing the ac signals to flow. We choose 1μF capacitors for this job, as the typical equivalent resistance of transistor circuits is often within an order-of-magnitude of 5 kΩ. Thus our high-pass filter has a low frequency $f_{-3\text{dB}} = \frac{1}{2\pi RC}$ — within an order of magnitude of 30 Hz.

(c) **Input and Output Impedances**

Recall that to measure an input impedance you place a variable resistor between the signal source and the amplifier input, whereas to measure an output impedance you use a resistor from output to ground. In either case the test resistance is adjusted until $\frac{1}{2}$ the original output is achieved. In either case the test resistance must not affect the biasing, thus a blocking capacitor must be in series with the test resistance when measuring impedances. (A blocking capacitor is always shown for the input; you must add one when measuring output impedance.). Note that if the output impedance is quite small, a larger blocking capacitor is needed (e.g., 6.8μF electrolytic). This is the case for the follower circuit. Additionally, small output impedance allows large output powers...so use power resistors when estimating the output impedance of the follower.

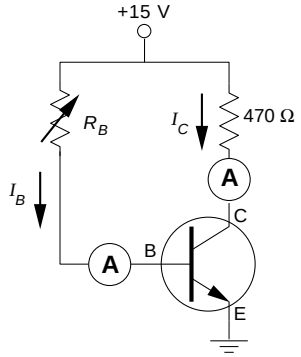


1. BJT Characteristics

   Select two different npn BJTs of the same device number (e.g., 2N3904). Using the web[1], obtain a characteristic curve for each, and secure them into your lab notebook. (Be gentle with the transistor leads, and keep track of which plot corresponds to which device.) From your characteristics, determine the *current gain* h_{fe} (also denoted β). Plug your device into the DMM transistor tester, and find its version of h_{fe}. Compare your values with the manufacturer's specifications.

2. Current Gain

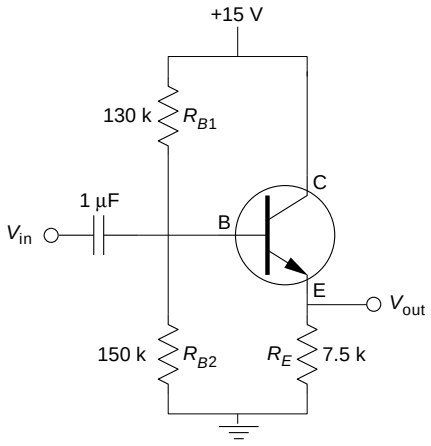
   Construct this circuit and measure the collector current, I_C, as a function of base current, I_B, for one of your transistors. Use the full range of R_B that produces 1 μA $< I_B <$ 0.3 mA. (Note: $I_B <$ 0.3 mA means $R_B >$ 50 kΩ...explain why!) Calculate the current gain, $h_{FE} = I_C/I_B$ (i.e., β), for each point. Note that the circuit limits the maximum value of I_C. Show how you could calculate $(I_C)_{\text{max}}$ from the circuit. Log-log plot[2] the current gain vs. I_C and compare with the results of part 1. Is β a constant? Note that β also depends on the device selected and temperature: In general, a circuit whose operation depends on a value of β is an unreliable (maybe inoperative) circuit!



[1] `http://block.physics.csbsju.edu`

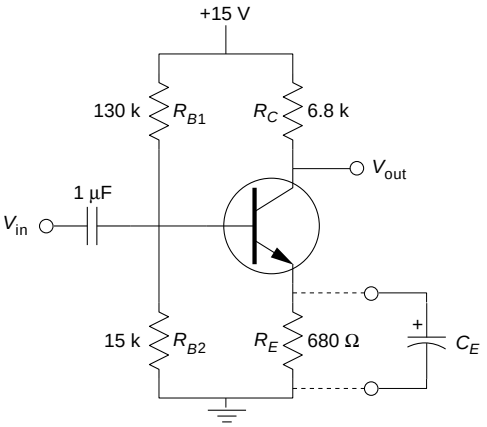
[2] `http://www.physics.csbsju.edu/plot` is what I'd use

3. Emitter Follower



Construct the amplifier shown, drive it with a sinusoidal wave at 10 kHz, and simultaneously observe the input and output waveforms on a scope. What is its ac gain? (Hence the name "follower.") Measure the base and emitter dc bias voltage levels and note whether they are what you expect them to be. Measure the amplifier's input impedance and compare it with your theoretical expectation. Using small resistors (e.g., 51 & 100 Ω and parallel combinations for yet smaller values), a 6.8μF blocking capacitor and very small amplitudes to avoid clipping, estimate the output impedance. Is it as expected?

4. Common-Emitter Amplifier



The amplifier shown at right illustrates the proper biasing method for a BJT common-emitter amplifier. Measure its ac voltage gain, input and output resistance, and compare them with theoretical predictions. Measure the high frequency $f_{-3\text{dB}}$ point. Now bypass the emitter resistor R_E with a 6.8μF electrolytic capacitor C_E and once more measure the ac gain and compare with the theoretical value. (Note that with C_E present, you will have to keep v_{in} very small to avoid clipping.)

CIRCUIT DESIGN: This circuit is designed to have a gain of 10. Given the gain, most resistor values follow immediately after specifying one resistor... e.g., for the output impedance. (This is unfortunate as it implies that we cannot separately set the input and output impedances.)

Generally speaking the output impedance of common emitter amps are within an order of magnitude of 5 kΩ. Here we determine that impedance by setting $R_C = 6.8$ kΩ. The gain of ten then requires $R_E = 680\ \Omega$. To have about 7.5 V across the transistor, we'll have 1 mA thru the 6.8k + 680 Ω = 7.48 k. The base bias is designed to have available $\sim 10\times$ the base current required to supply the 1 mA collector current: $(10/\beta)I_C$. The base voltage, V_B, should be about: $0.6 + 680\ \Omega \cdot 1\text{mA} = 1.3$ V. The the voltage divider resistances are determined from I_B and V_B:

$$R_{B1} = \frac{V_{CC} - V_B}{10 I_B} = \frac{13.7\text{ V}}{0.1\text{ mA}} = 137\text{ k}\Omega$$

$$R_{B2} = \frac{V_B}{9 I_B} = \frac{1.3\text{ V}}{0.09\text{ mA}} = 14.4\text{ k}\Omega$$

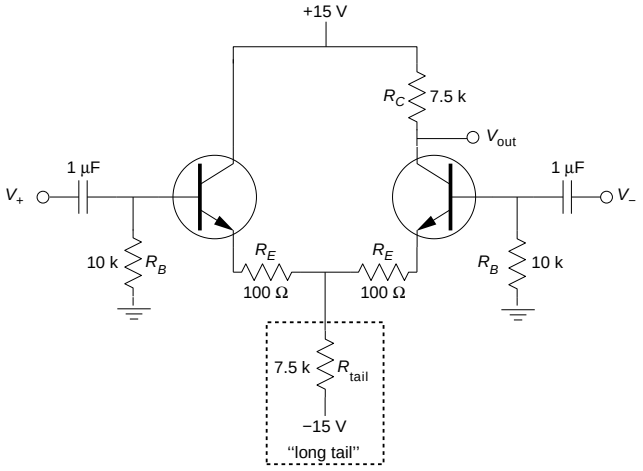
where we've assumed a conservative $\beta = 100$. using standard values, the input impedance of this circuit is: 130k‖15k‖β 680 Ω, i.e., about 11 k. The output impedance is about 6.8 k.

If $\beta \to \infty$ (i.e., zero current drawn from the voltage divider), the result is: $V_B = 1.55$ V, $I_C = 1.4$ mA and $V_{CE} = 4.5$ V. Whereas $I_C = .75$ mA, results in $V_{CE} = 9.4$ V and $V_B = 1.11$ V. Evidently $I_B = 33\ \mu$A to get that voltage droop (i.e., $R_{B1} \| R_{B2} \times 33\ \mu\text{A} = .44$ V), so $\beta = 23$. We conclude that over a wide range of β this circuit 'still works'[3]. Can you confirm these calculations?

[3]The definition of 'still works' depends on individual design requirements. In this case we've determined that at the extremes of $\beta \in (23, \infty)$ the maximum output voltage swing has been reduced from 7.5 V to about 5 V.

5. Differential Amplifier: "long-tailed pair" (H&H 2.3.8)

Using a "matched-pair" of 2N3904, construct the circuit shown. Note that one input (V_+) is a non-inverting input and the other (V_-) is an inverting input. Measure the circuit's differential gain by grounding one of the inputs and introducing a small signal into the other. Measure its common-mode gain by driving both inputs with the same signal (of, say, 1 V_{p-p}). From these data, compute this amplifier's CMRR. Note that H&H discuss this circuit (Fig. 2.64), where they derive:



$$G_{\text{diff}} = \frac{R_C}{2(R_E + r_e)}$$

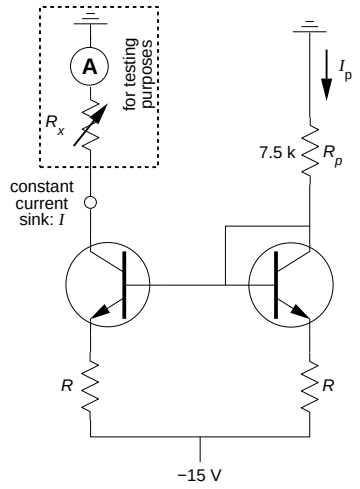
$$G_{\text{CM}} = -\frac{R_C}{2R_{\text{tail}} + R_E + r_e}$$

$$\text{CMRR} \approx \frac{R_{\text{tail}}}{R_E + r_e}$$

Compare these calculated gains to those you measured. Save this circuit!

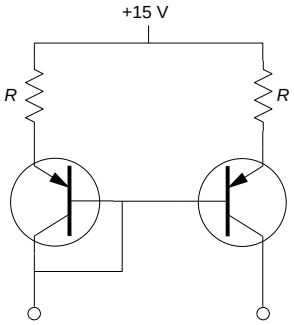
6. Current Mirror: active tail (H&H 2.3.7)

Construct the current mirror shown and report/explain the formula relating the "programming resistor" R_p to the constant current I. (Select R so that about 0.1–1 V drops across it for currents of a few mA—e.g., $\sim 200\Omega$). Check whether $I \sim I_p$ (as would be expected for identical transistors). Over what range of R_x is the current approximately constant? Try a new value for R_p and again measure both I_p and I. Warm one of the transistors with your fingers and note the effect this has on I. Discuss what determines the range of R_x values over which this circuit is useful. Finally remove all of the circuit in dashed boxes (i.e., R_x, ammeter, R_{tail}), return $R_p = 7.5$k and substitute the constant current sink for the long tail. Measure the differential amplifier's new differential and common-mode gains and compare the CMRR with its previous value in part 5. Comment on the change you observe.



7. PNP Current Mirror as active load—op amp's first stage

(Extra Credit) Construct a pnp current mirror using a matched pair of 2N3906. Plug the current mirror into the collectors of the matched pair transistors of #5. (Retain the current mirror tail; this pnp current mirror replaces both existing collector connections including R_C.) The resulting circuit is the first stage of many op amps. Sketch it in your lab notebook. Measure the amplifier's new differential and common-mode gains. The differential gain should be increased. Can you see how the current mirror makes "R_C" "infinite" for differential signals and "zero" for common-mode signals? Clipping even with no input may be a problem... a bias offset null would be helpful.



8. Complementary Push-Pull follower

This circuit is the basis of the output stage of most audio power amplifiers. Use a 2N3906 for the PNP transistor. Construct it, drive it with a large sinusoidal input, and observe the *crossover distortion* in V_{out} as you change both the amplitude and dc offset of V_{in}. Sketch the output and input when the input amplitude is about 3 V p-p with zero dc offset. Explain your observations. For zero offset in V_{in}, is crossover distortion more of a problem at large or small input amplitudes? (See H&H 2.4.1)