Note: A.C. voltages and currents are recorded here as rms quantities unless otherwise stated. (Your answers should also be rms quantities unless the problem requests otherwise.) Numerical answers should be reported with three significant digits.

1. Suppose three resistors (1 kΩ, 2 kΩ, and 3 kΩ) are connected in series and powered with a 12 V battery.

   (a) Draw a schematic diagram of the situation.

   (b) What current (in mA) flows from the battery? What power (in mW) is produced by the battery?

   (c) What is the voltage across each resistor? What is the current through each resistor?

2. Suppose three resistors (1 kΩ, 2 kΩ, and 3 kΩ) are connected in parallel and powered with a 12 V battery.

   (a) Draw a schematic diagram of the situation.

   (b) What current (in mA) flows from the battery? What power (in mW) is produced by the battery?

   (c) What is the voltage across each resistor? What is the current through each resistor?

3. Kirchhoff's Laws: See the below figures.

   (a) A current of 3 mA flows into one wire of a circuit consisting of 3 resistors, and 10 mA flows out another wire. Report the readings on the three voltmeters. Draw a schematic diagram showing which lead on each voltmeter is the 'red' lead.

   (b) An unknown device is connected in a circuit with a 9 V battery and a 15 kΩ resistor. The ammeter reads 0.5 mA. What does the voltmeter read?
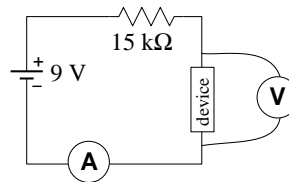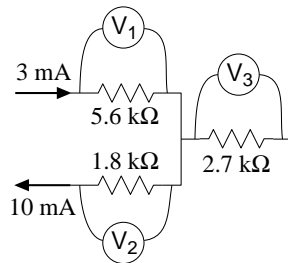
4. Which light bulb in the below left circuit shines the brightest? Why? Which light bulb shines the dimmest? Why?
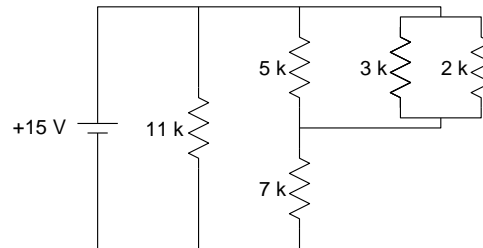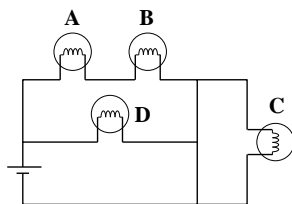

5. Consider the circuit diagrammed above right. Find the current flowing in each resistor. (Note: in this schematic (and many others) resistor values are listed without the Ω unit; "k" in this context means "kΩ".)

6. As shown right, a node is connected to three resistors (R_i). Each of the resistors connects to a known voltage (V_i). Show that the voltage at the node is:

$$V = \frac{\sum V_i G_i}{\sum G_i}$$

where the G_i are the conductances $G_i \equiv 1/R_i$. In short, the voltage at the node is the average of the voltages on the connections, weighted by conductances. (FYI: The result applies to any number of connections, not just three.)
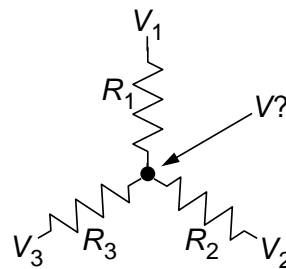
7. Consider the generic circuit shown (first—i.e., leftmost—of those shown right). Show that the current I through R_2 is a symmetric function of R_1 and R_2, that is swapping the values of R_1 and R_2 results in the same current. As a particular example of this result, in the two far right circuits the currents I_A and I_B must be equal.
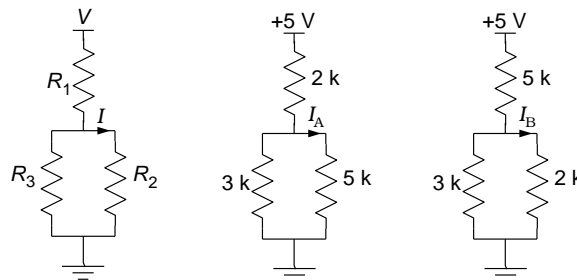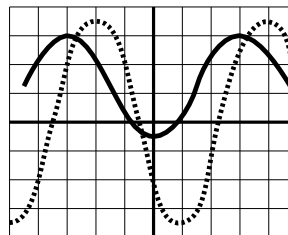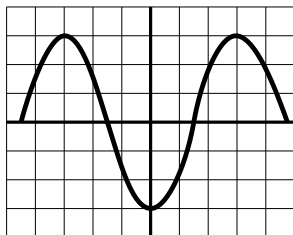
8. What is the (warm) resistance of a 100 W light bulb operating from a 120 V source?

9. The below left diagram shows a single sinusoidal scope trace. Determine: the peak-to-peak voltage, the voltage amplitude, the rms voltage, the wave period and frequency. Assume that the bottom of the scope display reads:

CH1 500mV   M 5.00ms   Ext ╱ 0.00V

10. The above right diagram shows a pair sinusoidal scope traces. Assume that the scope controls are set as in the previous problem with CH 2 (dotted) and CH 1 (solid) identical. Which trace is lagging: dotted or solid? What is the phase shift in degrees?

11. Manufacturers typically report DMM errors as a percentage of the reading plus a certain number of "digits". In this context, one digit means a 1 in the rightmost displayed digit and zeros everywhere else. Consider a DMM display: 0.707. Find the error in this reading if the device is:

   (a) METEX-3800 DC current, 2 mA range.
   (b) METEX-3800 AC current at 500 Hz, 2 A range.
   (c) Sinometer DM-97 resistance, 4 kΩ range.
   (d) Sinometer DM-97 AC volts at 200 Hz, 4 V range.

   The specification sheets can be found posted in the lab or in the manuals in the physics library. As always, errors should be rounded to one or two significant figures.

12. Work the previous problem assuming the display reads: 0.007

13. An a.c. voltage source follows the equation: $v(t) = A\sin(\omega t + \phi) + B$
    where $A = 5$ V, $B = 1$ V, $\omega = 1000$ rad/s, and $\phi = .45$ rad. Report values for the following:

    (a) average voltage (d.c. offset)

    (b) voltage amplitude

    (c) peak voltage

    (d) peak-to-peak voltage

    (e) rms voltage

    (f) voltage at $t = 0$

    (g) frequency

    (h) period

14. A function generator has an output impedance of 50 Ω and, when unloaded, produces a voltage amplitude of 10 V. What is the maximum (average) power that can be transferred to an external device attached to the function generator?

15. A circuit consists of an inductor (inductance L) connected directly to a 120 V, 60 Hz wall receptacle. What is the smallest L you could use and avoid blowing the 20 A fuse? A similar circuit consists of a capacitor connected directly to a wall receptacle. What is the largest C you could use and avoid blowing the fuse? In either case, the power company will bill you for 120 V×20 A = 2400 "Watts" of power. What is happening to all that "power"?

16. The dual scope trace in problem 10 was produced by a series RC circuit driven with a function generator (V_{in}, at some frequency f—the dotted curve in the scope trace of problem 10). The output, V_{out} is the solid curve in the scope trace. Both scope channels are on identical scales; you do not need the actual numerical values of the scope scales to answer the following questions.

    (a) Which signal is leading? What is the phase angle between V_{in} and V_{out}?

    (b) Is the output taken across the resistor or the capacitor? Provide a schematic diagram of the circuit. Is this a high-pass or low-pass filter?

    (c) Is f above or below $f_{-3\text{dB}}$? Calculate the ratio: $f/f_{-3\text{dB}}$

17. Express the following complex numbers in $r\angle\theta$ format (I bet your calculator can do this automatically):

    (a) $\dfrac{1}{1+i}$
    (b) $\dfrac{3+i}{1+3i}$
    (c) $25e^{2i}$
    (d) $(1/(1+i))^*$
    (e) $\left|\dfrac{1}{(1+i)}\right|$

18. Find the following in (a, b) format (I bet your calculator can do this automatically):

    (a) $\dfrac{3i-7}{i+4}$
    (b) $(.64 + .77i)^4$
    (c) $\sqrt{3+4i}$
    (d) $25e^{2i}$
    (e) $\ln(-1)$

19. In the below left circuit, find the voltage drop across each component and phase shift between that voltage and the current.
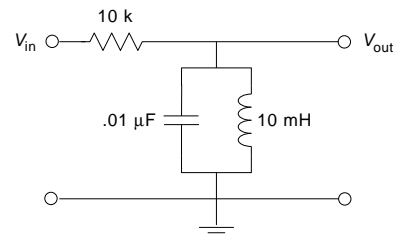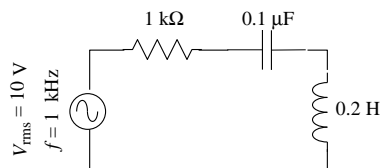
20. Consider the above right circuit. Plot V_{out} as a function of frequency, where $V_{\text{in}} = 10$ V. Plot the phase difference between V_{out} and V_{in} as a function of frequency. Your plotted frequency range should include frequencies such that $X_C \gg X_L$ and $X_C \ll X_L$. (Hint: if $z = Ae^{i\phi}$ for $A, \phi \in \mathbb{R}$, then in *Mathematica* A=Abs[z], and ϕ=Arg[z])

21. Work the previous problem again, but this time assume that the inductor is really a series combination of an ideal 10 mH inductor and a 100 Ω resistor. (Since inductors consist of a long thin wire wrapped into a coil, they typically have resistance in addition to inductance.)

22. Consider the below left high pass filter with: $V_{\text{in}} = 10$ V (at a frequency of 1 kHz), $C = .01$ μF, $R = 10$ kΩ. What is $f_{-3\text{dB}}$ for this filter? Find:

   (a) current flowing

   (b) voltage across R (V_{out})

   (c) voltage across C

   (d) the phase angle between V_{out} and V_{in}

Draw a scope trace diagram similar to problem 8, showing V_{in} (as a solid line) and V_{out} (as a dotted line). Report the scale settings (VOLTS/DIV and TIME/DIV) used in your sketch.
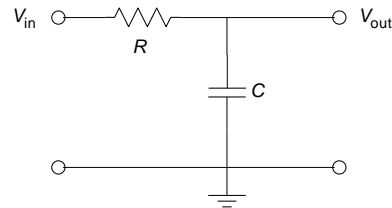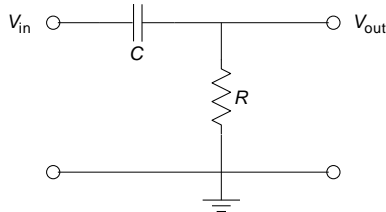
23. Consider the above right low pass filter with: $V_{\text{in}} = 0.1$ V (at a frequency of 1 kHz), $C = 6.8$ μF, $R = 50$ Ω. What is $f_{-3\text{dB}}$ for this filter? Find:

   (a) current flowing

   (b) voltage across R

   (c) voltage across C (V_{out})

   (d) the phase angle between V_{out} and V_{in}

Draw a scope trace diagram similar to problem 8, showing V_{in} (as a solid line) and V_{out} (as a dotted line). Report the scale settings (VOLTS/DIV and TIME/DIV) used in your sketch.

24. *LRC* Circuit

The circuit shown right includes two identical resistors (resistance R), an inductor (L), and a capacitor (C). Find the equivalent impedance, and show that if $R = \sqrt{L/C}$. the equivalent impedance does not depend on ω!
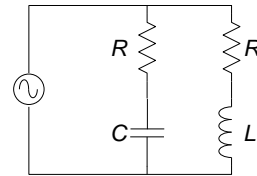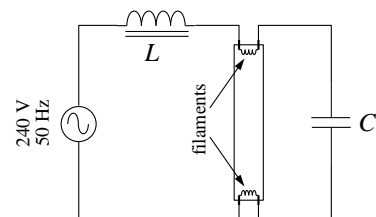
25. Fluorescent Lamp: run

In England (where the "mains" supply is 240 V at 50 Hz) fluorescent tubes are powered with the circuit shown. The inductor L ("ballast") is used as part of a voltage divider to supply the tube with less than 240 V. Consider the case of the T12 24" 20 Watt tubes used in our halls. When lit, these tubes draw 0.37 A. Assuming the tube acts just like a resistor, what is the voltage across the tube? What value of L would provide this current and voltage in England?
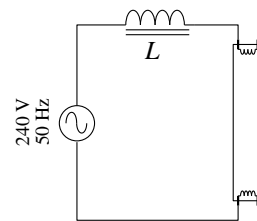
26. Fluorescent Lamp: *LRC* start?

In order to ignite the arc inside the fluorescent tube the filaments are heated (by sending a current through them) and then a high voltage pulse is applied. While not the usual method used, an *LRC* resonant circuit could be used to produce both a large filament current and a voltage well above 240 V, and thus facilitate the ignition. (The unlit tube acts is an insulator; the filaments are the R; use the value found in the previous problem for L.) If run exactly at resonance, what value of C is required? If the total filament resistance is 40 Ω how much current will flow? Find the voltage across the tube. Exact resonance would actually produce too much current. What value of C is required if the current is to be limited to 0.5 A?

27. Fluorescent Lamp: power factor

As in the previous problems, a 20 Watt fluorescent tube, when lit, will draw 0.37 A from the assumed 240 V supply. The power company will then bill you for 0.37 A × 240 V = 90 "Watts" whereas you are only using 20 W. Oddly enough you can reduce the current drawn from the receptacle by adding a capacitor in parallel to the tube+ballast. This "power factor correcting" capacitor results in a total impedance ($\mathbf{Z}_{\text{total}}$) that is real (i.e., the current drawn from the receptacle is in phase with the voltage). Show that the required C is given by:
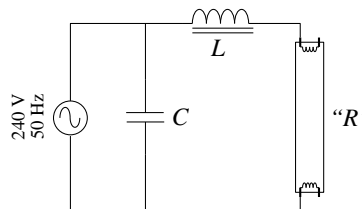
$$\omega RC = \frac{1}{\frac{R}{\omega L} + \frac{\omega L}{R}}$$

where R is the effective resistance of the tube. Calculate the value of C needed in England. Note: some algebraic tricks will give you a fast solution, however the tedious, but direct, approach of finding C to maximize $|\mathbf{Z}_{\text{total}}|$ (and hence minimize the current) will also produce the correct answer.

28. A homework problem describes a series LR circuit that is powered by a source producing a sine wave at 5 V_{rms}. Using the problem's component values and frequency a student calculates the current as $I = 5/(R + i\omega L)$ and gets $(12 - 5i)$ mA. Given all the proper components (inductor, resistor, properly adjusted function generator) and the the usual measurement tools available in our lab, report how this calculation could be confirmed by direct *measurement*. Note that lab DMMs report single rms values (related to the magnitude of the corresponding complex quantity) and that scopes provide a way to measure phase. Display the measurement results; explain how the results correspond to the calculated answer. Use schematics to show exactly how any measurement tools would be attached to the circuit.

29. Find the complex impedance of the RLC circuit shown to the right when it is driven by an angular frequency $\omega = 10^5$ s^{-1}. What voltage would an ac voltmeter placed between the terminals measure? What current would an ac ammeter measure if connected between the two terminals (careful)?
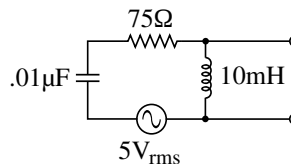
30. The circuit to the right is driven by a 12 V rms sinusoidal waveform at a frequency of 1000 Hz.

    (a) Calculate the (complex) voltage at A; Calculate the (complex) voltage at B.

    (b) For the two terminals A & B the equivalent ac Thévenin voltage should just be the difference between the voltage at A and voltage at B. Find this value.

    (c) Calculate the (complex) Thévenin impedance, $\mathbf{Z}_{TH}$

    (d) Find a resistor/capacitor combination that, at this frequency, has the same impedance as you found above in c.

    (e) If terminals A & B are connected by a 1 kΩ resistor what (complex) current would flow through it? Express it in both complex rectangular and magnitude-phase form.
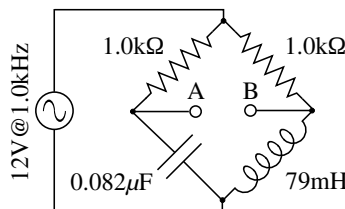
31. A function generator (output: 5 V_{rms} at a frequency of 3500 Hz) powers the circuit shown right. The ammeter (A) and voltmeters (V) shown in the circuit are ideal and like, ordinary DMMs, they report rms values.

    (a) Find the complex current I; report its magnitude and phase. Does the function generator's voltage lead or lag I?

   (b) Report the three values found by the three meters.
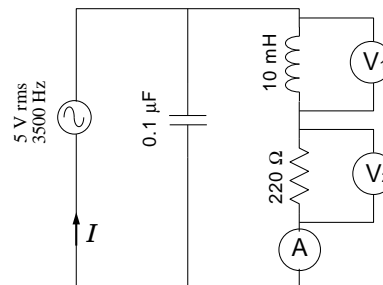
32. The circuit shown below right is driven with an ideal 3 V_{rms} source at 2.5 kHz. The ammeter (A) and voltmeter (V) shown in the circuit are ideal and, like ordinary DMMs, report rms values.

   (a) Find the complex current I; report its magnitude and phase. Does the function generator's voltage lead or lag I?

   (b) Find the values reported by the two meters. (Hint: think voltage divider.)
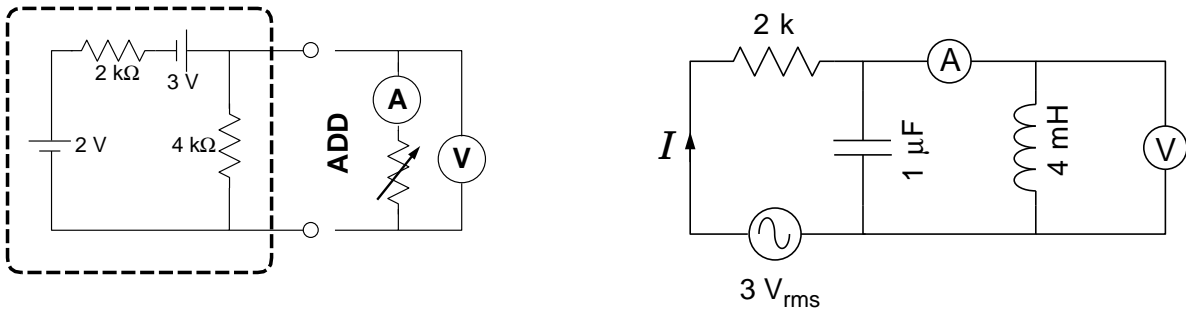
33. Find the Thévenin equivalent circuit for the two terminals connected to the circuit inside the dashed box as shown above left. The variable resistor+ammeter+voltmeter circuit shown adjacent is then connected to the two terminals. (A) If the variable resistor is set to infinite resistance, what would the voltmeter and ammeter read? (B) If the variable resistor is adjusted until the voltmeter reads exactly one half the open-circuit voltage across the terminals, what is the resistance of the variable resistor? (C) If the variable resistor is adjusted to 10× the Thévenin resistance of the boxed circuit, what would the voltmeter and ammeter read?

34. Find the Thévenin equivalent circuits for the below circuits. (The circles show the terminal locations.)
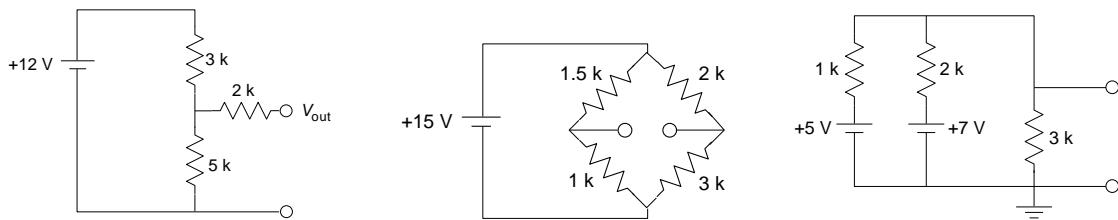

35. Find the Thévenin equivalent circuit for the below left circuit—the parts inside the dashed box. A 1 V battery is attached to the two terminals. Will this battery charge or discharge? How much current will flow? Sketch the equivalent circuit you determined above now with the 1 V battery attached to the two terminals.
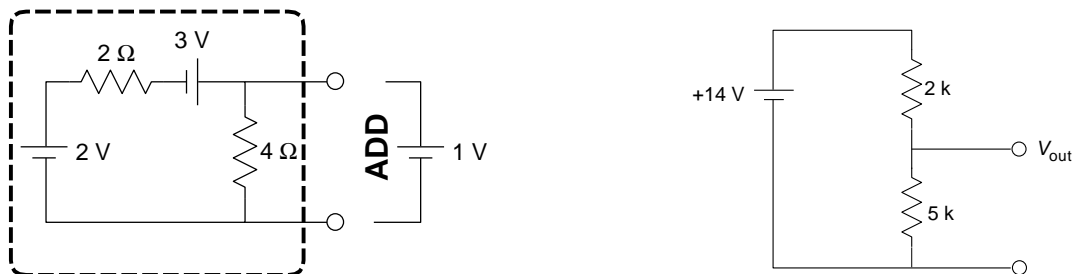

36. Find the Thévenin equivalent circuit for the above right voltage divider and use your equivalent circuit to answer the following questions:

   (a) What is V_{out} with nothing connected between the terminals?

   (b) What is V_{out} with a 6 kΩ resistor connected between the terminals?

   (c) When an unknown resistor is connected between the terminals, V_{out} is found to be 50% of what was found in part (a). What is the value of the unknown resistance?

   (d) When an unknown resistor is connected between the terminals, V_{out} is found to be 80% of what was found in part (a). What is the value of the unknown resistance?

37. You are trying to understand the behavior of a device with two terminals. When you measure the voltage between the two terminals with a digital voltmeter you get 5 V. When you attach a 200 Ω resistor between the two terminals you measure 4.5 V between the terminals. Calculate component values for a Thévenin equivalent circuit for the device and draw that equivalent circuit. If you attach a 50 Ω resistor between the terminals, how much power will be dissipated in the resistor?

38. Norton's theorem is the sidekick of Thévenin theorem; it states that any two terminals in a complex circuit with batteries, resistors, current sources, etc., acts exactly like a resistor and current source connected in parallel between the two terminals. (As in the diagram below.) What is the Thévenin equivalent circuit for a Norton circuit? (I.e., find the Thévenin V and R for the below circuit. Be sure to explain your solution!)
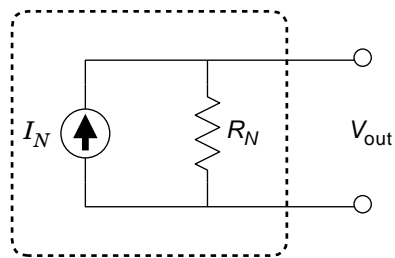

39. Suppose you want to build a battery eliminator for a small portable radio. The radio normally draws 30 mA from four AA (penlight) cells (which are connected in series). You are willing to accept a peak-to-peak ripple of 0.2 V, and plan to use a simple bridge rectifier circuit with a transformer powered by the wall receptacle (and no voltage regulator). Draw your circuit!

   (a) What voltage transformer (rms) should you purchase?
   (b) What size filter capacitor should you purchase?

40. For each of the four power supply circuits shown below, find the output d.c. voltage. (All the transformers produce an rms output voltage of 6.3 V; note that the last transformer is center tapped.) For both circuits on the left: if $C = 4700\ \mu$F and a d.c. current of $I = 0.5$ A is being drawn from the power supply, report the d.c. droop and a.c. ripple.
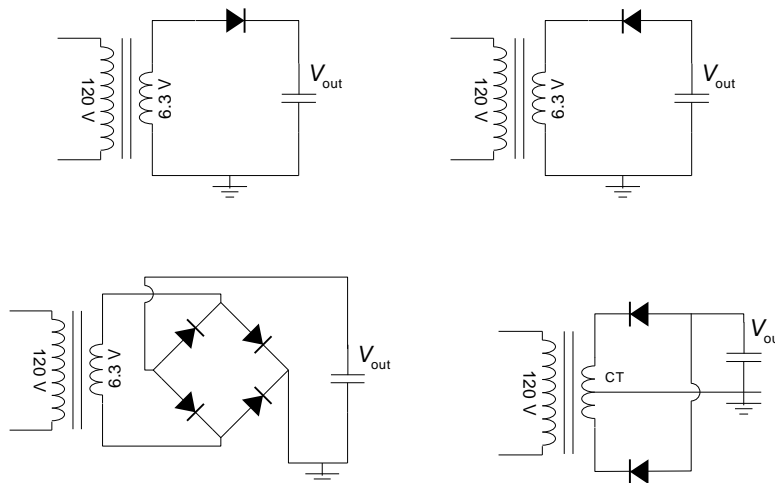

41. You want to make battery-based power supply for a digital (+5 V) circuit that draws 0.5 A. A 7805 voltage regulator will be used to reduce the battery's voltage to the required +5 V. Common high-capacity, lead-acid batteries come in 12 V and 6 V versions. Which must you use? How much power (heat) will be dissipated in the 7805?

42. In lab you have made +5 V power supplies by voltage dividing a +15 V supply and by using a 7805. How is the 7805 power supply superior to the voltage divider power supply?

43. Generic Amplifier I — Thévenin applied

The following two problems deal with a
generic amplifier (see right) with voltage
gain A, input impedance R_{in}, and output
impedance R_{out} driven with a sine wave
input.
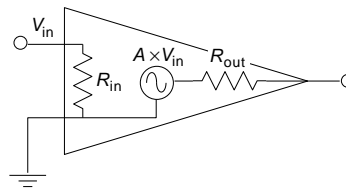
(a) A function generator with an output impedance of 50 Ω, and a 8 Ω speaker are to be connected to
the input and output of the amplifier (see below left). The amplifier has a gain of 30 dB with an
input impedance of 150 Ω and an output impedance of 16 Ω). The function generator is connected
to a scope and its output is adjusted to 0.2 V peak-to-peak. Assuming the speaker acts exactly
like an 8 Ω resistor, find the power dissipated in the speaker.
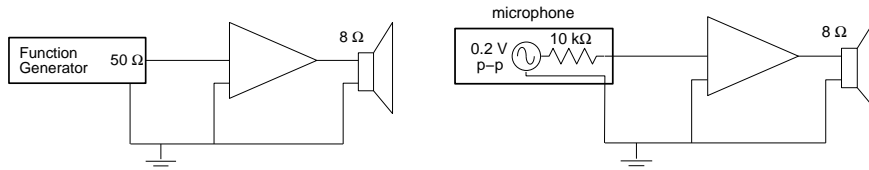
(b) A microphone with a Thévenin equivalent circuit of a 0.2 V peak-to-peak voltage source in series
with 10 kΩ, drives the above circuit instead of the function generator. Find the power dissipated
in the speaker.

(c) The same microphone drives a unit-gain (A=1) amplifier with an input impedance of 1 MΩ and
an output impedance of 1 Ω. Find the power dissipated in the speaker.

(d) If the microphone is directly connected to the speaker, what power will be dissipated in the
speaker? Why does direct connection produce less output power than the follower?

44. Generic Amplifier II — Thévenin applied

(a) Consider a circuit that consists of three identical generic amplifiers (gain: A, input impedance:
R_{in}, output impedance: R_{out}) cascaded together. What is the formula for the open-circuit voltage
gain of the circuit?
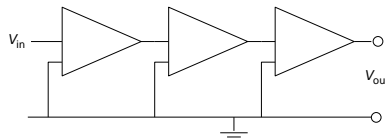
(b) Assume that two identical amplifiers (gain 10, input impedance 1 kΩ, output impedance 100 Ω)
are capacitively coupled with a 0.1 μF capacitor (see below, left). What is the high frequency
open-circuit gain of the system? At low frequency the gain will be less. At what frequency will
the gain be 3 dB less than at high frequency?
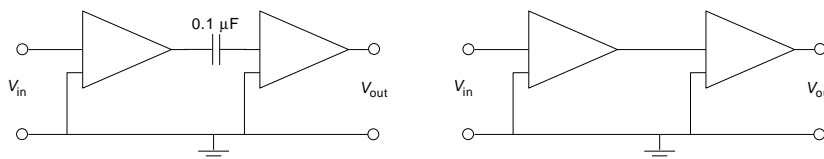
(c) Two identical amplifiers are directly-coupled as shown above right. The amps have an input
capacitance of 200 pF, output resistance of 100 Ω, and gain of 10. What is the low frequency
open-circuit gain of the system? At high frequency the gain will be less. At what frequency will
the gain be 3 dB less than at low frequency?

45. Given a function generator, resistance substitution box (variable resistor), generic amp, and scope
connected to the generic amp's output, describe how you could measure R_{in} in lab. Draw a schematic
diagram showing the circuit used to measure R_{in}. Describe the process and draw a schematic diagram
showing the circuit used to measure R_{out}.

46. Bode Plot slope: dB/octave

The given Bode Plot (a log-log plot of attenuation as a function of frequency) looks like a straight line (and hence is a power law: attenuation=Af^B). What is the slope of this line in dB/octave? What is the corresponding power B?

Bode Plot
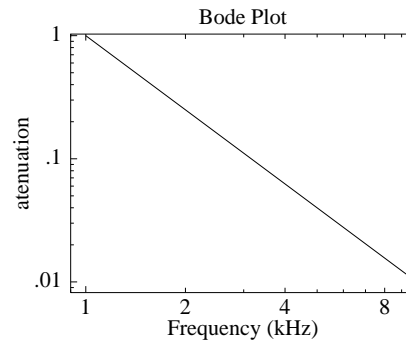
47. In the below left diagram, assume the op-amp is ideal. Report: V_{out} and the the voltmeter and ammeter readings.
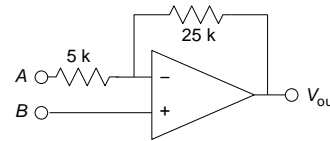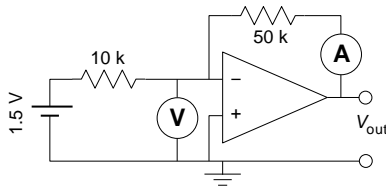
48. In the above right diagram...

   (a) If B is grounded and A is used as the amplifier input, what is the voltage gain (including sign) and the input impedance?

   (b) If A is grounded and B is used as the amplifier input, what is the voltage gain (including sign) and the input impedance?

49. Design an inverting amplifier circuit with an input impedance of 5 kΩ and a gain of -20.

50. Design a multiple op-amp circuit that performs the following bit of arithmetic with voltage sources A, B, and C.
$$V_{\text{out}} = A + 2B - 3C$$

51. The circuits shown right show the results of applying various inputs to a differential amplifier.

   (a) What is the differential (or normal mode) gain?

   (b) What is the common-mode gain?

   (c) What is the Common Mode Rejection Ratio (CMRR)?

   (d) Express the CMRR in terms of dB.
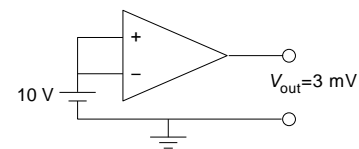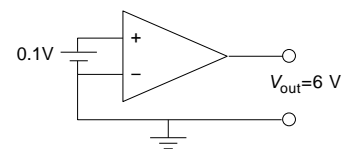
52. 411 Op-amp

In the circuit displayed to the right, the op-amp is a 411. What is $f_{-3\text{dB}}$ for this circuit? (Hint: HH Figure 4.47 p. 247). What is the output impedance at $f_{-3\text{dB}}$. (For additional sources on 411 see previous problem.) What is the input impedance?
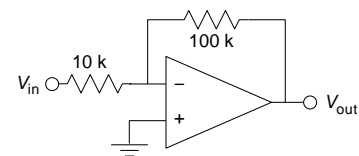
53. For each of the below circuits built with ordinary op-amps, indicate with a lower-case letter any and all of the following properties that apply to it.

(a) High input impedance ($> 5\text{M}\Omega$)

(b) Low input impedance ($< 5\text{k}\Omega$)

(c) Inverting amplifier

(d) Non-inverting amplifier

(e) Absolute value of gain is 10 ($\pm 1\%$)

(f) Follower

(g) Differentiator

(h) Integrator

(i) This circuit won't work (explain briefly why)
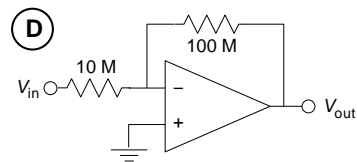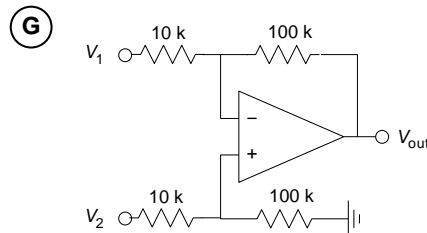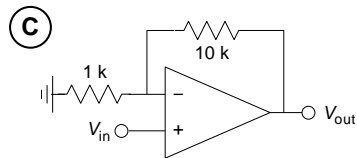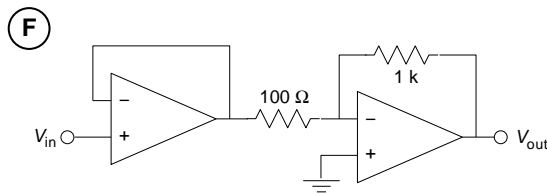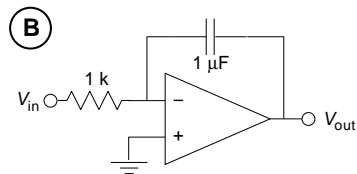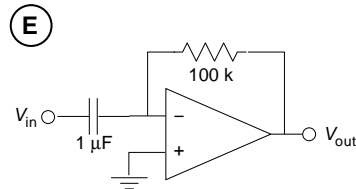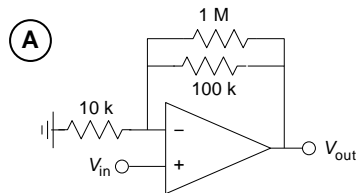
54. Constant current source

In lab you built the circuit to the right using a 411 and ± 15 V power supplies. The basic specs of a 411 can be found HH p. 271; many characterizing plots can be found p. 246–7, 251; the official datasheet is in the class web site. Calculate the expected ammeter reading. Calculate the largest R_L for which the current is constant. If the 180 Ω resistor were replaced with a 18 Ω, what problem would occur? If the 1 k resistor were replaced with a 4.7 k, would a problem occur?
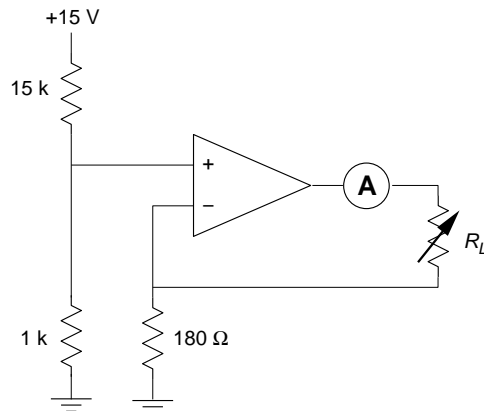
55. One way of making a sinusoidal output, is to start with an easily produced wave shape (square or triangle) and filter out—as much as possible—the harmonics. The Fourier series (which shows the harmonic content) of symmetrical, unit-amplitude square and triangle waves are:

$$\text{square} \;=\; \frac{4}{\pi} \sum_{n=1,3,5\ldots} \frac{1}{n}\, \sin(n\omega t)$$

$$\text{triangle} \;=\; \frac{8}{\pi^2} \sum_{n=1,3,5\ldots} \frac{(-1)^{(n-1)/2}}{n^2}\, \sin(n\omega t)$$

Assume that $f_{-3\text{dB}}$ is set to the fundamental ($n = 1$) frequency and the aim is to reduce the next (non-zero) harmonic amplitude (here, $n = 3$) to 1% of the fundamental's amplitude. Specify the dB/octave required to do this job for (a) the square wave and (b) the triangle wave. (Hint: start by finding how many octaves $3f$ is above f.)

56. A full-wave rectified signal (of the usual $f = 60$ Hz line voltage, where below $\omega = 2\pi f$) has the Fourier series:

$$\text{full-wave} = \frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6\ldots} \frac{1}{n^2 - 1}\, \cos(n\omega t)$$

The aim is to reduce the $n = 2$ (i.e., 120 Hz) amplitude to 1% of the dc voltage level using a simple RC filter (at 6 dB/octave). Find the filter's $f_{-3\text{dB}}$. Note: in the usual circuit (with diodes and a capacitor, and with no current draw), the capacitor holds the peak value of the rectified wave (here 1) rather than the average value (here $2/\pi$).

57. Design a 555 oscillator producing a tone of frequency 440 Hz. Make a schematic diagram of your design (and be sure to report how every pin on the 555 is connected).

58. A 555 is connected as an oscillator (e.g., HH Fig. 7.9, p. 429) using a 0.1 μF capacitor and two 1 kΩ resistors, and powered with +10 V.

  (a) What is the frequency of of the resulting oscillations?

  (b) Make a moderately accurate sketch of of the output signal (pin 3) as a function of time.
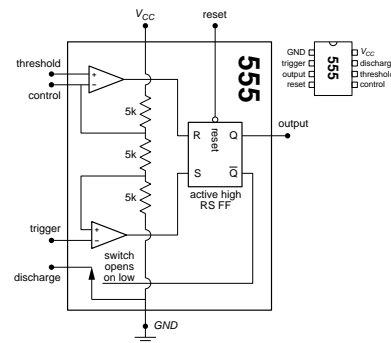
59. The *duty cycle* of an asymmetrical square wave is usually defined as the ratio of the time the signal is high to the overall period of the wave.

  (a) Find a formula, expressed in terms of the resistor values, for the duty cycle of a 555 (as an oscillator) .

  (b) Your formula should suggest that making one resistor 0 Ω would make a symmetrical square wave (duty cycle of 50%). Why is this a bad idea?

60. n-channel JFET and Ohmmeter

  (a) Two resistance measurements (A and B) are made sequentially with one ohmmeter following the connections as shown in the diagram to the right. The + (red) terminal is connected exactly as shown. Each reading is expected to be either a "small" resistance (say, < 5 kΩ) or a "large" resistance (say, > 5 MΩ). For each connection, report which will be observed and why.

  (b) Suppose now (in both cases) the + and – (red and black) ohmmeter leads are swapped. For both situations, report whether the new readings are "small" or "large" and why.
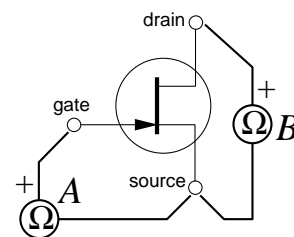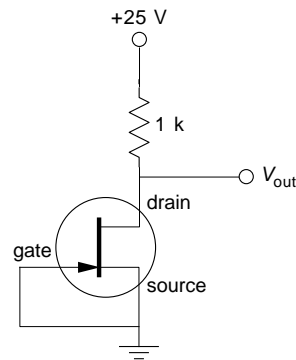
61. nJFET Characteristic Curves[1]

The file `fet4.pdf` on the class web site contains the characteristic curves of an n-channel junction field-effect transistor (nJFET). Each characteristic curve is labeled with the corresponding gate voltage (V_G). Using the plot estimate the zero-gate-voltage drain current (I_{DSS}) and gate source cutoff voltage (V_{TO} or $V_{GS,\text{off}}$, a.k.a. pinchoff voltage V_P). This FET is to be used in the circuit to the right. Directly on hardcopy of `fet4.pdf`: draw the load line for this circuit and label "Q" your selected quiescent point. What d.c. gate voltage is required for your Q point (i.e., gate bias voltage)? If the gate voltage is 0.5 V above your gate bias voltage, what drain current (I_D) and drain-source voltage (V_{DS}) would result? If the gate voltage is 0.5 V below your gate bias voltage, what I_D and V_{DS} would result? Use this result to calculate the gain of the circuit (i.e., a 1 V peak-to-peak input at the gate results in what peak-to-peak output signal at the drain).

+15 V

I_D 1.2 k

drain V_{DS}

V_G gate source
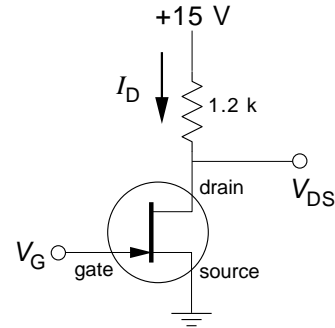
62. n-channel JFET I_{DSS}

The n-channel junction field-effect transistor (nJFET) used in the circuit to the right has the characteristic curves recorded in the file `fet4.pdf` on the class web site. Each characteristic curve is labeled with the corresponding gate voltage (V_G). Report the voltage V_{out} (relative to ground).

+25 V

1 k

V_{out}

drain

gate

source

63. Variable (voltage-controlled) Gain Amplifier

The file `fet4b.pdf` on the class web site contains the *small* V_{DS} characteristic curves of an n-channel junction field-effect transistor (nJFET). Each characteristic curve is labeled with the corresponding gate voltage (V_G). This FET is used in the circuit to the right.

(a) If $R_1 = 10$ kΩ and $V_G = 0$ V, what is the gain of this circuit?

(b) If $R_1 = 10$ kΩ and $V_G = -1.5$ V, what is the gain of this circuit?

(c) If $R_1 = 100$ kΩ and $V_G = 0$ V, what is the gain of this circuit?

V_{in} V_{out}

R_1

V_G
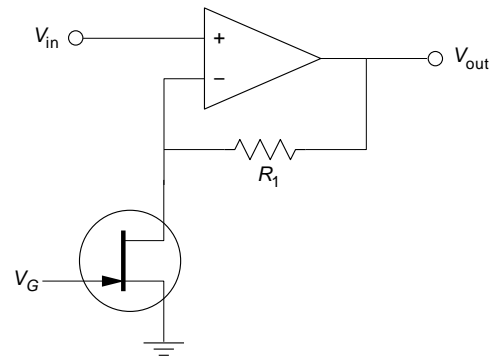
64. Consider the common source FET amplifier shown right:

(a) Somebody claims the ammeter reads 20 mA. Explain why this is impossible and report what the ammeter should read if the circuit is properly designed. (Assume this current in answering the remaining questions.)

(b) What is the gate bias voltage?

(c) If the transconductance is 0.01 ℧, what is the gain?

(d) What is the input impedance?

(e) What is the output impedance?
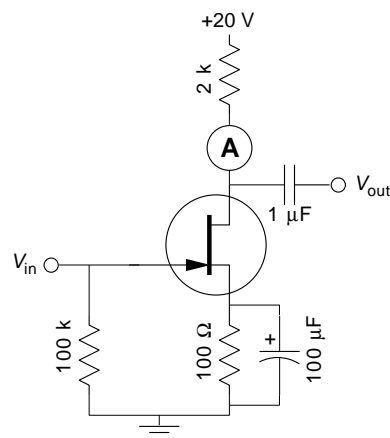
+20 V

2 k

A

V_{out}

1 μF

V_{in}

100 k   100 Ω   100 μF

65. A common source amplifier (see below right) is to be built using an n-channel JFET with the characteristic curves shown below left. For each component of this amp, report a value and how that value was determined (often just a formula). Report your gate bias voltage, transconductance at that voltage, amplifier gain and input and output impedances.


Characteristic Curve for FET
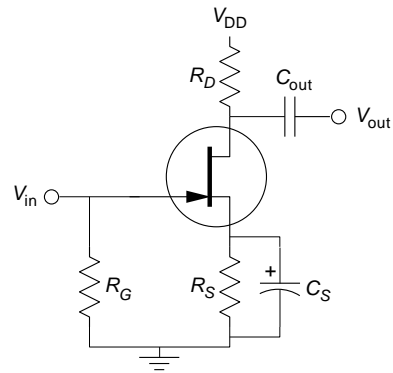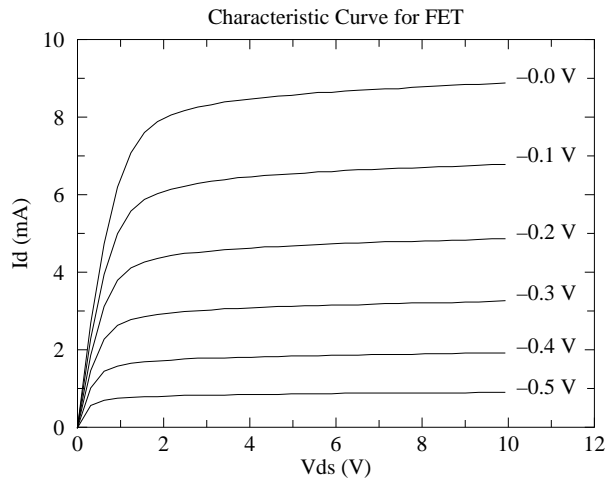
66. Three resistance measurements (A, B, and C) are made sequentially with one ohmmeter as shown in the diagram to the right. The + (red) terminal is connected exactly as shown. For each connection, report whether the ohmmeter reports a "small" resistance (say, < 5 kΩ) or a "large" resistance (say, > 5 MΩ). Report the basis for your expectations.
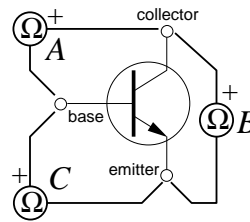
67. In the circuit shown below left, V_{out} is 5 V. What is h_{FE} (a.k.a. β)? How much power is dissipated in the transistor?
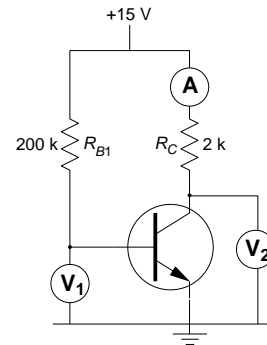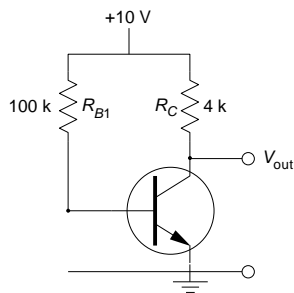

68. In the circuit shown above right, h_{FE} is 80. Report the reading expected on the voltmeters V_1 and V_2 and the ammeter A. If h_{FE} is 160, what will the meters report?

69. Assuming that the transistor shown has $h_{FE} = 50$, find V_{out} for the below circuits. If the transistor turns out to have $h_{FE} = 100$, find the new values of V_{out}.
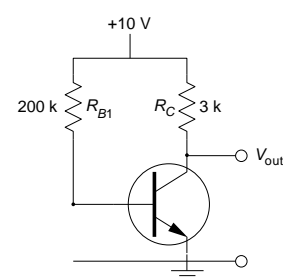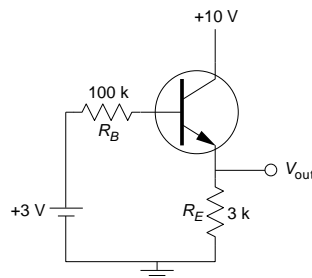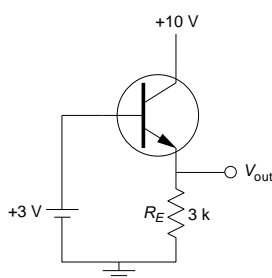
70. In the circuit shown right, the transistor has $h_{FE} = 150$. The amplifier should have a low frequency response that extends down to 60 Hz. Calculate:

(a) the base current

(b) the collector current

(c) r_e

(d) the collector-emitter voltage

(e) the voltage gain

(f) C_{in}

(g) C_{out}
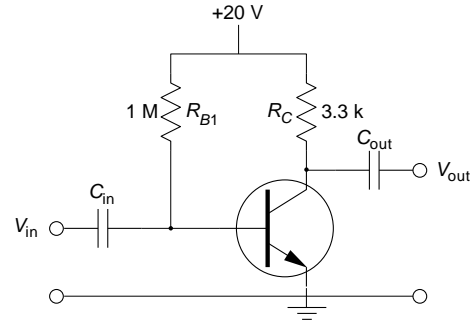
71. In the circuit shown right, begin by assuming that the transistor's $h_{FE} = \beta$ is so large that the base current can be neglected.

(a) Calculate the voltages at B, E, and C, and the collector current I_C.

(b) If the base current is *not* negligible, how will the voltages at B, E, and C be affected? That is for the points B, E, and C, report if the voltage will increase, decrease, or stay the same.

(c) If I_C is less than that found in (a) and as a result V_C is changed by 1 V, find V_E, V_B, and I_C.

(d) Report the Thévenin equivalent circuit for the 8k+2k voltage divider. If the voltage divider is in fact producing the output voltage given by V_B in part (c), how much current must the divider be sourcing?

(e) If the base current is given by that found in part (d) and the collector current is given by that found in part in (c), what is the β of the transistor?

(f) Repeat the calculation of the previous part, but this time assume that the voltage divider is 80k+20k.
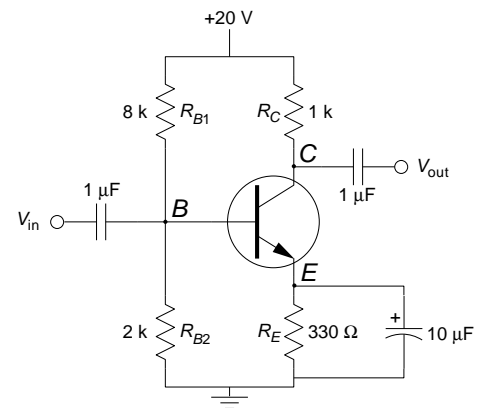

72. Design a BJT amplifier using the circuit shown right. You should provide all component values and the calculations that support those values. (This will require a choice of the frequencies to be amplified.) Calculate the input and output impedance. The circuit constraints are: voltage gain of 20, output impedance < 5 kΩ, input impedance > 15 kΩ, and that your base bias circuit will work for a transistor with $\beta = 100$ or $\beta = \infty$.
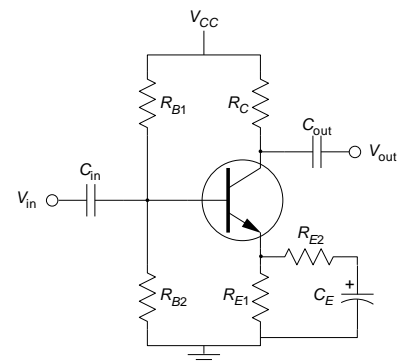
73. Design a BJT amplifier for a gain of 10 and an output impedance of 5 kΩ (i.e., find all the values for the components shown). Design the base bias assuming $\beta = 150$. Assume the amplifier is to be used for audio frequencies in the range 20–20,000 Hz. Calculate the input impedance.

How robust is your design, that is, how small could your actual transistor β be and still have the circuit work? Assume that the actual transistor used results in a V_E just 70% of your design V_E (this would often cause problems), and then calculate the actual transistor's β.
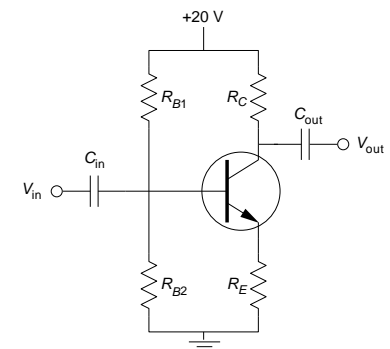
74. Biasing—Voltage Divider Design: Using a supply voltage ($V_{CC} = V_{\text{in}} = 20$ V) you aim to provide a base current of $I_B = 20$ μA at a base voltage of $V_B = V_{\text{out}} = 2$ V (and hence emitter voltage $V_E = 1.4$ V) for a BJT amplifier as in problem 73. The impedance looking in the base is expected to be $\beta \times R_E = 100 \times 700$ Ω, and the current, I_E, through R_E is expected to be $V_E/R_E = 2$ mA. For a well designed circuit we expect $V_{CE} = \frac{1}{2}V_{CC}$, however if the actual V_E does not match the designed V_E, V_{CE} will be changed with:

$$\Delta V_{CE} = -(R_E + R_C)\Delta I_E$$

or, dividing by the designed $V_{CE\,\text{design}} = \frac{1}{2}V_{CC}$, we have:

$$\frac{\Delta V_{CE}}{V_{CE\,\text{design}}} \approx \frac{-\Delta I_E}{I_{E\,\text{design}}} = \frac{-\Delta V_E}{V_{E\,\text{design}}}$$

where we've used $I_{E\,\text{design}} = \frac{1}{2}V_{CC}/(R_E + R_C)$. Main point: transistor variations can easily lead to variations in V_E of $\Delta V_E \sim .2$ V; if $V_{E\,\text{design}}$ is 'small' (say, less than a volt) the result can be big deviations from $V_{CE\,\text{design}}$. We may make stiff biasing voltage dividers to mitigate this result (but that hurts the input impedance). Below you investigate the impact of variations in transistor β on ΔV_E for a couple of bias design methods.

A. Method A: As suggested by H&H, design the voltage divider with a Thévenin equivalent resistance of $\frac{1}{10}\times$ the impedance looking in the base and a Thévenin equivalent voltage of the desired V_B. With this bias design, the design $V_B = V_{\text{out}}$ is only achieved with zero I_B, i.e., $\beta \to \infty$, but, because of the impedance mismatch, V_{out} should be 'close' to the designed value even when $I_{B\,\text{design}}$ is sourced.

V_{in}

i. Find the required R_1 and R_2.

ii. If 20 μA is drawn from V_{out}, what is the resulting V_{out}?

iii. What is the resulting ΔV_E and $\Delta V_E/V_{E\,\text{design}}$?

R_1

iv. If 40 μA is drawn from V_{out}, what is the resulting $\Delta V_E/V_{E\,\text{design}}$?

B. Method B: Design the voltage divider so that $V_{\text{out}} = 2$ V, with $10\times I_B$ through R_1 and $9 \times I_B$ through R_2 (and an assumed $1 \times I_B$ exiting through V_{out}).

V_{out}

i. Find the required R_1 and R_2.

R_2

ii. If $\beta \to \infty$, in fact no current would exit at V_{out} and as a result V_{out} would rise above 2 V. Find V_{out} in this circumstance. What is the resulting $\Delta V_E/V_{E\,\text{design}}$?

iii. If 40 μA is drawn from V_{out}, what is the resulting $\Delta V_E/V_{E\,\text{design}}$?
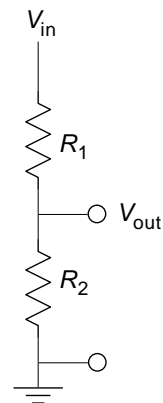
75. (a) The following page has characteristic curves for BJT and FET. Directly on the NPN characteristic curves, label the region where the transistor is saturated, on, and off. Draw the schematic diagram symbol for a PNP bipolar transistor and label each lead with its proper name.

(b) Directly on the n-channel characteristic curves, label the ohmic region, the region where the FET is cut-off (a.k.a. sub-threshold), and where the FET is active. (Note: what I call an "active" FET, is often called "saturated" or "pinched-off". Of course, "saturated" for a FET is different from "saturated" for a bipolar.) Draw the schematic diagram symbol for a p-channel FET and label each lead with its proper name.

76. Consider the below characteristic curves of an npn bipolar transistor. Calculate $h_{fe} = \beta$. Assume the npn transistor is part of a common emitter amplifier with a supply voltage of 12 V. Directly on the below plot, draw in the load line for a 2 kΩ collector resistor, and mark a nice operating point Q. At Q, what is the change in the collector voltage ΔV_{CE} for a change in the base current $\Delta I_B = .01$ mA? Calculate h_{ie} using your operating point's base current. What change in the base voltage ΔV_{BE} will accompany the change in the base current $\Delta I_B = .01$ mA? Calculate the ac voltage gain: $\Delta V_{CE}/\Delta V_{BE}$. At your operating point, how much power is dissipated in the transistor?

Characteristic Curves for NPN
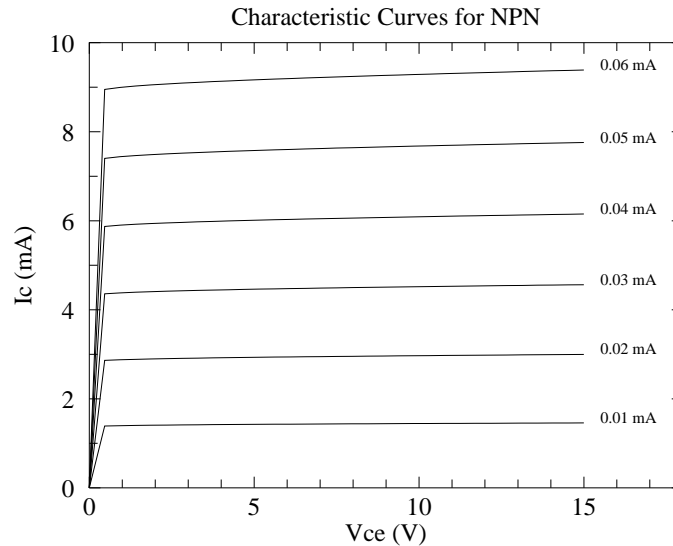
77. Consider the below characteristic curves of an n-channel JFET. What is I_{DSS}? Calculate g for $V_{GS} = -1.5$ V. Estimate the threshold gate voltage. Assuming a supply voltage of 12 V, draw directly on the below plot the load line for a 2 kΩ drain resistor characteristic curves. Label Q the operating point obtained with $V_{GS} = -1.5$ V. What is the quiescent drain current? How much power is dissipated in the transistor in this quiescent state? Design a common source amplifier (see problem 59) using this FET. Your schematic diagram of the circuit should show all component values and input and output locations. As usual, you will bias the gate (here to $V_{GS} = -1.5$ V) using a source resistor (bypassed with a capacitor C_S so the ac signal doesn't see it). What value of C_S should you use if the amplifier is to amplify signals with frequencies between 100 and 10,000 Hz? Report the expected voltage gain and both input and output impedance.

Characteristic Curves for nFET
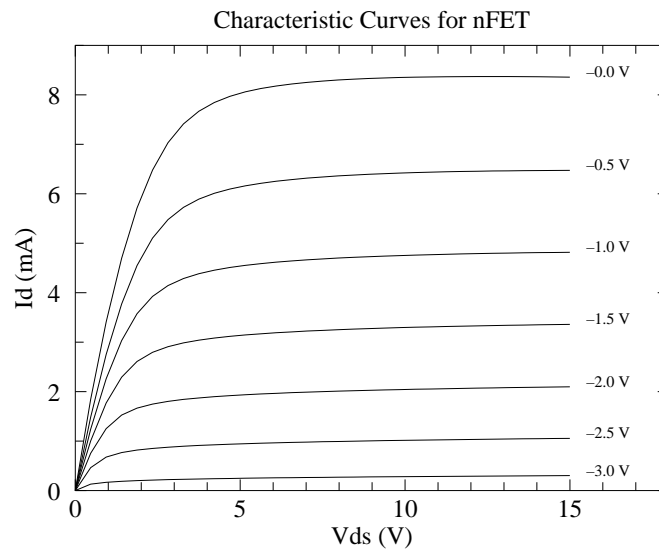
78. Describe briefly what each of the below circuits does.
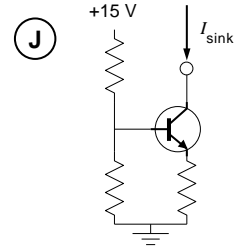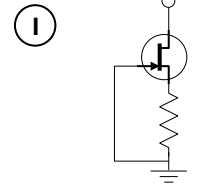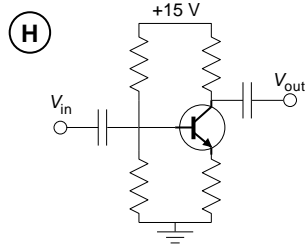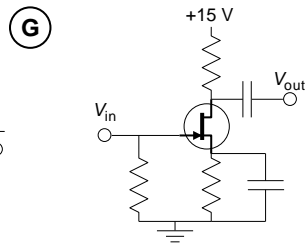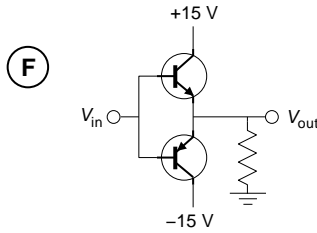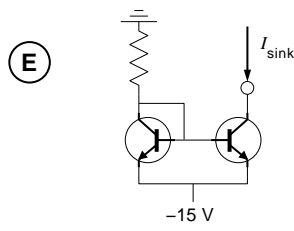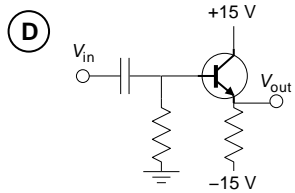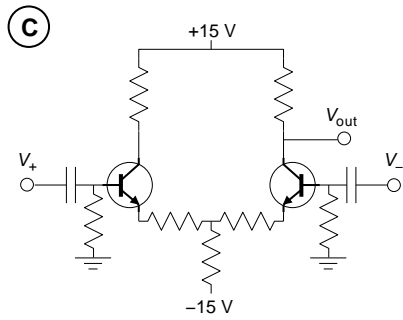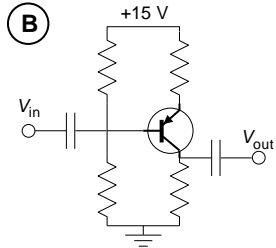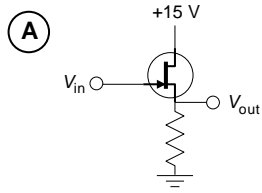
79. Define the following electronic terms:

A. no-load	a. common mode rejection ratio
B. current source	b. slew rate
C. open circuit & short circuit	c. open loop gain
D. pot	d. differential amplifier
E. choke	e. "rail-to-rail"
F. condenser	f. virtual ground
G. Norton/Thévenin	g. amplifier $f_{-3\text{dB}}$
H. input/output impedance	h. biasing
I. lead/lag	i. blocking/bypass capacitor
J. Bode plot	j. active load
K. Wheatstone bridge	k. FET, MOSFET
L. xy scope mode	l. n-channel, p-channel
M. Coupling▶AC (scope)	m. enhancement/depletion
N. full-wave/half-wave rectification	n. drain/gate/source
O. bridge rectification	o. "common" in e.g., common source amp
P. center-tapped transformer	p. admittance: y_{fs}, y_{os}
Q. linear power supply	q. g, transconductance
R. switching power supply	r. Bipolar transistor (NPN, PNP)
S. load regulation	s. collector/base/emitter
T. voltage droop (power supply)	t. hybrid parameters: h_{fe}, h_{oe}, h_{ie},
U. stiff (voltage source)	u. h_{ie} vs. r_e
V. diode cathode/anode	v. β, current gain
W. PN junction	w. current mirror
X. p-type/n-type material	x. push-pull
Y. minority carrier	y. Darlington
Z. negative feedback	z. cascode